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Improved Contacts And Device Performance In Mos2 Transistors Using 2d Semiconductor Interlayers

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IMPROVED CONTACTS AND DEVICE PERFORMANCE IN MoS_2 TRANSISTORS USING 2D SEMICONDUCTOR INTERLAYERS

by

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DISSERTATION

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DEDICATION

To my family, friends, and everyone who has provided support along the way

"The fact that we live at the bottom of a deep gravity well, on the surface of a gas covered planet going around a nuclear fireball 90 million miles away and think this be normal is obviously some indication of how skewed our perspective tends to be."

-Douglas Adams

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LIST OF ABBREVIATIONS

2D	Two-Dimensional
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
BEUV	Beyond Extreme Ultraviolet
BP	Black Phosphorus
CMOS	Complementary Metal-Oxide Semiconductor
CNL	Charge Neutrality Level
CVD	Chemical Vapor Deposition
DIBL	Drain Induced Barrier Lowering
EBL	Electron Beam Lithography
EUV	Extreme Ultraviolet
FET	Field-Effect Transistor
FinFET	Fin Field-Effect Transistor
FLP	Fermi Level Pinning
GAAFET	Gate-All-Around Field-Effect Transistor
GaAs	Gallium Arsenide
Ge	Germanium
hBN	Hexagonal Boron Nitride
HDMS	Hexamethyldisilazane
HfO_2	Hafnium Oxide
IC	Integrated Circuit
IPA	Isopropanol

MEK	Methyl Ethyl Ketone
MgO	Magnesium Oxide
MIBK	Methyl Isobutyl Ketone
MIGS	Metal Induced Gap States
MIS	Metal-Insulator Semiconductor
MoS_2	Molybdenum Disulfide
$MoSe_2$	Molybdenum Diselenide
$MoTe_2$	Molybdenum Ditelluride
MSS	Metal-Semiconductor-Semiconductor
nMOS	n Metal-Oxide Semiconductor
NPGS	Nanopattern Generation System
PC	Polycarbonate
PDMS	Polydimethylsiloxane
$PdSe_2$	Palladium Diselenide
PEB	Post-Exposure Bake
PMMA	Polymethyl Methacrylate
pMOS	p Metal-Oxide Semiconductor
PR	Photoresist
PVD	Physical Vapor Deposition
SB	Schottky Barrier
SBH	Schottky Barrier Height
SCE	Short Channel Effect
SEM	Scanning Electron Microscope

Si	Silicon
SiO_2	Silicon Oxide
SS	Subthreshold Swing
Ta_2O_5	Tantalum Oxide
TiO_2	Titanium Oxide
TLM	Transfer Length Method
TMD	Transition Metal Dichalcogenide
UTB-FET	Ultra-Thin Body Field-Effect Transistor
UV	Ultraviolet
vdW	van der Waals
WS_2	Tungsten Disulfide
WSe_2	Tungsten Diselenide

Chapter 1 BACKGROUND AND MOTIVATION

1.1 Field-Effect Transistors

Over the past half-century, integrated circuits (ICs) have revolutionized technology, playing a role in nearly all modern electronic devices. At the heart of an IC lies the field-effect transistor (FET). A FET is a three-terminal device consisting of a drain, source, and gate. A typical silicon (Si) FET is structure is fabricated on a substrate with heavily doped drain/source regions. A dielectric material (e.g. silicon oxide; SiO_2, hafnium oxide; HfO_2) is deposited or grown (SiO_2 is typically thermally grown while some other oxides like HfO_2 are deposited using atomic layer deposition) in the region of the substrate spanning the heavily doped drain and source. Metal is subsequently deposited over the drain/source regions as well as the dielectric material, functioning as the drain/source electrodes and the gate electrode, respectively. There are two types of basic Si-FETs: *n*- or *p*-Si FETs. Here, the discussion will focus on *n*-Si FETs (or nMOS), for *p*-Si FETs (or pMOS) the principle is the same, but the *n*- and *p*-doping is interchanged. For example, an *n*-Si FET is fabricated with a *p*-Si substrate and heavily *n*-doped drain/source regions as shown in ***Figure 1.1*(a)**.

A FET operates based on two distinct electric fields. The transverse electric field develops as a result of the applied potential difference between the gate and the substrate, known as the gate voltage, V_{GS}. The lateral electric field arises due to the application of a non-zero source to drain potential, V_{DS}, and is the primary mechanism driving current flow in the FET. Consider a device initially in the off-state, where the gate-voltage is much less than the voltage needed to induce a channel (i.e. the threshold voltage), $V_{\mathrm{GS}} \ll V_{\mathrm{TH}}$, and a non-zero source/drain voltage, $V_{DS} > 0$ (for *n*-Si FETs). In this

case, the drain and source regions form forward and reverse biased *p*-*n* junctions with the substrate preventing a substantial flow of current, contributing to low off-state current. When the gate voltage is increased, but still below the threshold voltage, the transverse electric field produced by the gate penetrates further into the substrate. This electric field repels majority holes (in the case of a *p*-Si substrate) from the surface, creating a depletion region near the surface. A portion of the depletion region is assisted by the drain/source *p*-*n* junctions, the depletion charge in the would-be channel region is balanced by charge in drain/source regions. In addition, some minority electrons are attracted to the surface, but at these low gate voltage values their concentrations are not enough to cause much effect. As the gate voltage is increased further, the transverse electric field continues to repel majority holes from the surface while attracting minority electrons to the surface. At some gate voltage value, the threshold voltage is reached where an inversion layer is formed. Here the inversion layer dominates over the intrinsic substrate doping levels. The inversion layer is a dense concentration of electrons that extends from the source to drain regions and forms the conductive channel of the FET as shown in ***Figure 1.1*****(b)**. Once the threshold voltage is reached, the lateral electric field drives current flow from the source to drain and further increasing the gate voltage only increases the density of the inversion layer.

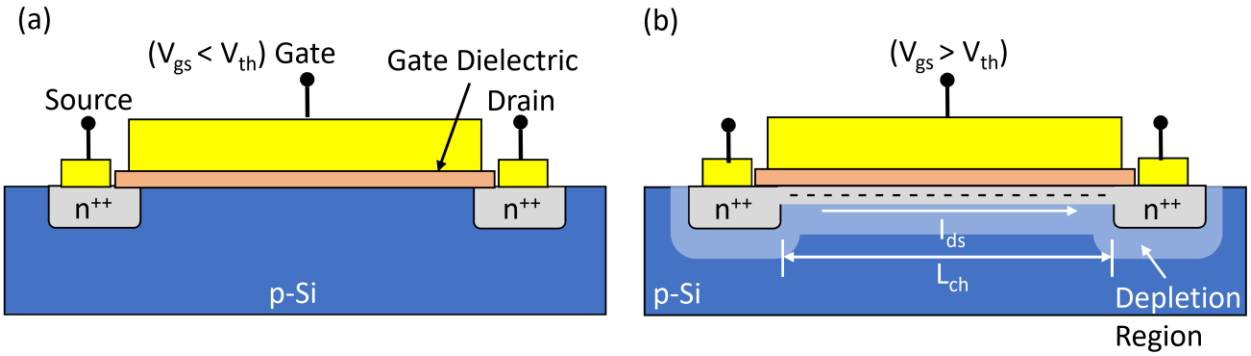

Figure 1.1 Basic schematic of 3D FET and operation. **(a)** Schematic of nMOS device with heavily n-doped drain and source regions and gate dielectric in the off-state. **(b)** As the gate voltage is increased, the holes present near the surface are repelled by the application of a positive gate voltage (and its resulting electric field). Further application and increase in the gate voltage yields a depletion region beneath the contacts and a small concentration of electrons near the surface. Once the threshold voltage is reached, a conductive channel of electrons is formed that extends from the source and drain and defines the channel length over which current can flow.

The ICs used in digital, analog, and memory circuits require increasingly larger transistor density to enable low-power and high-speed devices. Until recently, Moore's observation that computing power doubles every two years has held and has been facilitated by large increases in the number of transistors.[1] To accommodate the need for larger densities, the FETs that compose the ICs have been increasingly miniaturized. In the 1970s transistor sizes were on the order of several microns with densities near one-hundred thousand transistors per chip.[2, 3] While in 2018, commercial transistor sizes had decreased substantially to less than ten nanometers and the densities had skyrocketed to well over a billion transistors per chip.[4] In less than 50 years the transistor size has decreased nearly three orders of magnitude while the density has increased by over five orders of magnitude.

Increasingly miniaturized devices come at a cost, however. Decreased transistor size requires increasingly complex fabrication processes, often requiring the development of new equipment and techniques to help facilitate these processes. For example,

resolution in photolithography, an integral process in IC fabrication is limited by the diffraction limit. To reach resolutions adequate for the 10 nm technology node new techniques such as extreme ultraviolet (EUV) and beyond extreme ultraviolet (BEUV) lithography are being explored.[5] Aside from fabrication challenges, there are much more pressing issues in terms of the physical consequences of transistor scaling.

In order to properly scale devices, various FET parameters must be scaled simultaneously to ensure proper device function. Generally, this is to keep the internal electric fields constant.[6] As the device size is decreased, and the channel length transitions from the long-channel to the short-channel regime, the potential distribution in the channel begins to depend on both the x and y - directions. To mitigate this effect, the device parameters must be changed in concert with one another. For example, if the device length (L) is scaled by a factor of κ, then so should the device width (W), junction depths (x_j), and oxide thickness (t_{ox}). ***Table 1.1*** summarizes some the scaling factors for FETs, known as Dennard scaling factors.[7] However, as device geometries have decreased substantially since the advent of these scaling rules it has been difficult and impractical to maintain them. The primary reason for this is that these ideal scaling rules are impeded by other factors that are fundamentally not scalable. Parameters like the channel doping (N_{A}) cannot be scaled indefinitely without fear of *p*-*n* junction breakdown or the contact junction depth cannot be scaled indefinitely without sacrificing low-resistance at the contact interface.[6] If devices are not scaled properly, then issues begin to emerge that adversely affect device operation, known as short channel effects (SCEs).

Device or Circuit Parameter	**Scaling Factor**
Device dimension t_{ox}, L, W, x_j	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$

Current *I*	$1/\kappa$
Power dissipation *VI*	$1/\kappa^2$

Table 1.1 Device scaling rules for FETs.

Suppose that in a short channel device, the channel thickness is not scaled properly (i.e. the scaling has not followed the rules laid out in ***Table 1.1***), and the drain/source junction depths are too deep. This can cause unintended electrostatic interactions between the source and drain. The inversion and depletion layers are primarily created by the transverse electric field applied by the gate; however, the drain/source regions also work to balance some of the depletion charge. For long channel devices, the percentage of depletion charge balanced by the drain/source regions is small compared to the charge depletion induced by the gate. As the channel length is decreased, however, the drain/source regions balance a greater percentage of depletion charge. This effect, known as drain induced barrier lowering (DIBL), lowers the potential barrier to the channel and alters the threshold voltage of the device. ***Figure 1.2*** shows the effect that decreasing device geometry has on the depletion region sizes at the drain and source. In the extreme case of DIBL, the depletion regions beneath the drain and source can merge, exhibiting a phenomenon known as punch-through, rendering the device inoperable. Obviously, alterations in the threshold voltage and other unintended SCEs are undesirable for reliable device operation. While there are some actions that can be taken to prevent DIBL, such as anti-punch-though implants, or reducing the drain/source junction depth, these still do not protect against SCEs indefinitely.[3] Structures or materials that can mitigate SCEs would be ideal while still maintaining the ability to miniaturize devices.

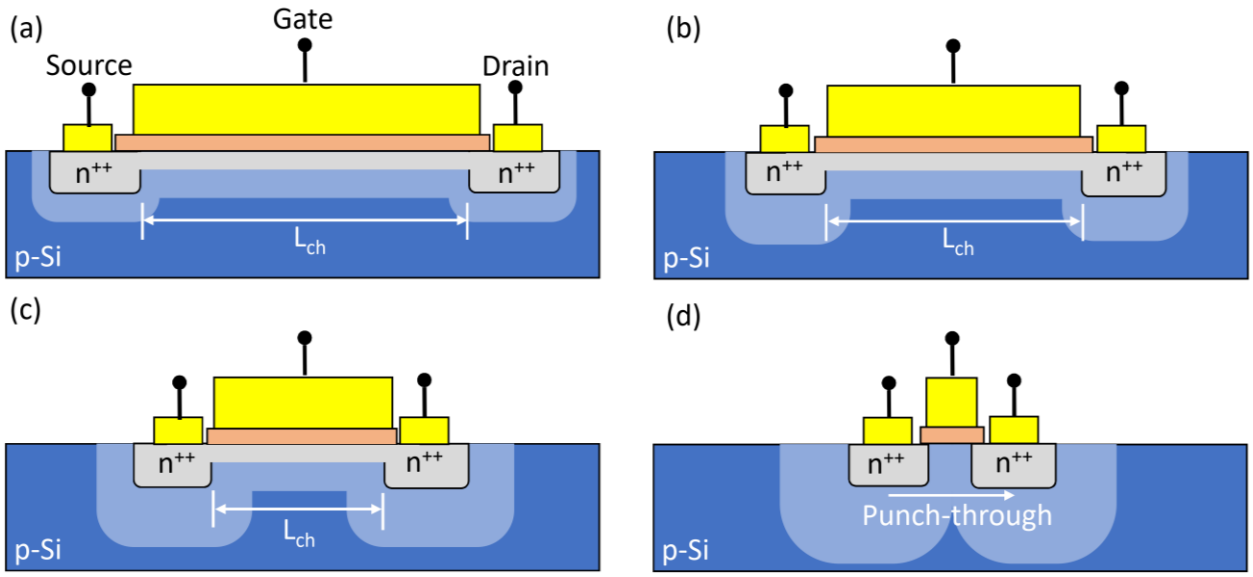

Figure 1.2 Illustration of decreasing device geometry and its effects on operation. In a sufficiently **(a)** long channel device, operation occurs as normal. **(b)** When the device size begins to shrink, the depletion region size increases and a **(c)** further decrease in size yields a larger depletion region size. In each case, the threshold voltage may be altered due to DIBL and the device may turn on prematurely. **(d)** At the limit, the depletion regions at each contact merge and punch-through occurs rendering the device inoperable.

Since the breakdown of Dennard scaling and the deviation from the scaling rules, new device structures have been sought. This is a consequence of SCEs, as discussed above. Smaller device sizes result in a less electrostatic control. Control of device operation is governed by the potential distribution $\Phi(x, y)$ in the channel, which according to Poisson's equation is given by

$$\frac{d^2\Phi(x,y)}{dx^2} + \frac{d^2\Phi(x,y)}{dy^2} = \frac{qN_A}{\epsilon_s}, \qquad (\mathbf{1.1})$$

where x is defined over the channel length ($0 \leq x \leq L$) and y is defined over the channel thickness ($0 \leq y \leq t_s$), N_A is the channel doping, and ϵ_s is the dielectric constant of the channel material. Assuming the following boundary conditions: (i) the electric field at $y = 0$ is determined by the capacitance of the gate, (ii) the electric field at $y = t_s$ is essentially

zero, and (iii) the potential at the bottom of the channel is some constant function in the x-direction (i.e. $\Phi(x,0) = c_0(x)$).[8] It can be shown that ***equation (1.1)*** can be reduced to

$$\frac{d^2\Phi}{dx^2} = \frac{\Phi}{\lambda^2}. \qquad (\mathbf{1.2})$$

The quantity λ is defined as the natural scaling length, and in a conventional FET design is defined as

$$\lambda = \sqrt{\frac{\epsilon_s}{\epsilon_{ox}} t_s t_{ox}}, \qquad (\mathbf{1.3})$$

where ϵ_s and ϵ_{ox} are the dielectric constants of the semiconductor and gate oxide material, respectively, and t_s and t_{ox} are the thicknesses of the semiconductor channel and oxide, respectively.[8] This term is central to the understanding of how the changes in the channel thickness affect the electrostatic potential in the channel. The natural scaling length represents the amount of electrostatic control the gate has over the potential in the channel. As the channel length is decreased, the natural scaling length must also be decreased to compensate for the changes in the electric field in the channel. ***Equation (1.2)*** can be solved by defining the potentials at the drain ($x = L$) and source ($x = 0$), such that

$$\Phi(0) = V_{bi} - \Phi_{gs} + \frac{qN_A}{\epsilon_s}\lambda^2 = \Phi_s, \qquad (\mathbf{1.4})$$

$$\Phi(L) = V_{ds} + V_{bi} - \Phi_{gs} + \frac{qN_A}{\epsilon_s}\lambda^2 = \Phi_d, \qquad (\mathbf{1.5})$$

where V_{bi} is the built-in potential at the *p-n* junctions between the heavily doped source/drain and the channel, Φ_{gs} is the potential due to the applied gate voltage, and V_{ds} is the applied drain/source potential. To study the behavior under extreme SCEs, the minimum potential in the channel should be found. Making the assumptions that the

channel length is much larger than the natural length scale ($L/\lambda \gg 1$), maintaining the long-channel regime, the minimum channel potential is

$$\Phi_{min} = 2\sqrt{\Phi_s \Phi_d} e^{-L/2\lambda}. \quad (\mathbf{1.6})$$

In the long-channel limit, basically a device free from SCEs, the solution is $\Phi = 0$. As the device size decreases, to obtain to minimize SCEs the potential minimum in the channel should be as close to zero as possible. The primary parameter for achieving this is to have a large ratio between the channel length and natural scaling length (L/λ). Maintaining an effective ratio between L and λ determines whether the gate is still in dominant control of the channel or if SCEs dominate.[9] Since the minimum channel potential decays exponentially with L/λ, a relatively small change in this ratio has a large effect on the minimum channel potential, and $\mathrm{L}/\lambda \approx 5 - 10$ is usually sufficient, and any resulting SCEs are tolerable if $\mathrm{L}/\lambda > 2$.[8, 10, 11]

In essence, smaller λ represents reduced SCEs. Based on ***equation (1.3)***, there are several possible ways to decrease λ in a conventional FET design. Much research has been devoted to the idea of achieving higher dielectric constants of the gate dielectric material.[12, 13] In addition, decreasing the gate oxide thickness, is another avenue that has been pursued, but without precautions, there is a significant issue of gate leakage as the gate oxide thickness is decreased. In terms of the conventional FET design it is also possible to reduce the channel thickness, which has been explored in ultra-thin body FETs (UTB-FETs).[14, 15] However, UTB-FETs made from reduced channel material thicknesses suffer from increased surface roughness scattering due to bandgap nonuniformity, and any would-be performance improvement is degraded.[16, 17]

Conventional FET structures with Si have seemingly run their course and to continue scaling new device architectures have been realized. One such device structure that is now commercially used is the FinFET.[18] The FinFET has a gate wrapped around the channel and is a form of the aptly named gate-all-around FET (GAAFET). By employing this design, the natural scaling length equation is altered to give:[19]

$$\lambda = \sqrt{\frac{\epsilon_s}{2\epsilon_{ox}}\left(1+\frac{\epsilon_{ox}}{4\epsilon_s}\frac{t_s}{t_{ox}}\right)t_s t_{ox}}. \qquad (\mathbf{1.7})$$

In wrapping the gate around the channel, the natural scaling length is decreased by nearly 10%, indicating an increase in the amount of electrostatic control achieved and thus a reduction in SCEs. Recent production of FinFETs with an equivalent channel length of 7 nm have been realized and 5 nm nodes are expected in the coming years.[4] However, FinFETs are increasingly complex to fabricate and are still susceptible to SCEs. Based on this, continued miniaturization of FETs faces an imminent roadblock, while new fabrication processes and device configurations can prolong the current paradigm, ultimately, new materials must be sought.

Let us briefly quantitatively discuss the extreme limits of the scaling lengths and its relationship to channel size for a conventional FET and FinFET device structures. Suppose a thin hafnium oxide (HfO_2) gate dielectric ($\epsilon_{ox} = 25$) is used ($t_{ox} = 4$ nm).[16] The channel material in a conventional FET and FinFET structure ($\epsilon_s = 11.9$), for the reasons discussed above, cannot be thinned down to atomic thicknesses without severe degradation of device performance and thus we will assume a thickness limit of $t_s = 5$ nm.[20] With these parameters, the natural scaling length for a conventional FET is $\lambda_{FET} = 3.09$ nm and $\lambda_{FinFET} = 2.81$ nm for a FinFET. Keeping with the requirement that $L/\lambda \geq 2$,

these scaling lengths imply that the minimum channel lengths possible to avoid severe device susceptibly to SCEs for a conventional FET and FinFET are $L_{\text{FET}} = 6.2$ nm and $L_{\text{FinFET}} = 5.6$ nm. Notably, achieving these extreme regimes would require significant advances in the current semiconductor processing techniques, adding increasingly complex fabrication steps, but at least provide a superficial picture for the ultimate limits achievable in the future with traditional semiconductor materials.

Ultimately, the limiting factor in scaling in traditional semiconductor materials is the channel thickness. Consider, instead, a set of materials whose thickness could be thinned to one atomic layer ($t_s = 0.65$ nm) without suffering from the bandgap nonuniformities that degrade UTB-FETs. Using this newly identified low-dimensional set of materials with a HfO_2 gate oxide with a thin oxide thickness ($t_{ox} = 4$ nm), a greatly reduced natural scaling length of $\lambda_{\text{low-D}} = 0.64$ nm. This is a significant decrease in the scaling length compared to that possible for conventional FETs and FinFETs. Similarly, the minimum channel length achievable in such a material with this scaling length is $L_{\text{low-D}} = 1.3$ nm. If a set of materials could be identified that could achieve this scaling range, then the ability to deal with SCEs in extreme length scales would be greatly improved. The ability to mitigate SCEs in this regime would allow for the continued growth of transistor technology for many decades to come.

1.2 Two-Dimensional Materials and Transition Metal Dichalcogenides

In the pursuit of identifying new materials immune to SCEs, two-dimensional (2D) materials have emerged as a promising candidate. 2D materials differ from other typical semiconductor materials (e.g. Si, GaAs, Ge) in that they are layered materials. As a result, they can be easily cleaved down to single atomic layers.[21] Another important structural

aspect of 2D materials is that they are free from dangling bonds and also maintain excellent bandgap uniformity which means that, unlike the UTB-FETs discussed in the previous section, they are not susceptible to increased out-of-plane scattering when decreasing the material thickness. Based on this, 2D materials have quickly gathered much attention for next-generation electronics in the post-silicon era.

The properties exhibited in 2D materials range from insulators, topological insulators, semiconductors, semimetals, metals, and superconductors.[22-24] With such a wide-range of material properties the list of potential applications for 2D materials is long and includes flexible nanoelectronics, spintronics, optoelectronics, and low-power digital electronics.[25-30] The 2D materials era was started by the isolation of graphene and the demonstration of high electrical conductivity, mechanical strength, and thermal and chemical stability in it.[21, 31] Initially, graphene caused much excitement due to its stunning properties, but this optmizism quickly faded as it was shown that graphene was not a semiconductor material, it lacked an instrinsic bandgap, essential for use as a channel material in digital electronics.[32] Efforts were made to induce a bandgap in graphene, and while this was moderately successful, the resulting performance was severely degraded, causing the loss of many of the impressive qualities sought after in devices.[33, 34] As a result, graphene, as a potential channel material in next-generation digital electronics was discarded. The focus then turned to other 2D materials that possess properties similar to graphene but also have a suitable intrinsic bandgap.

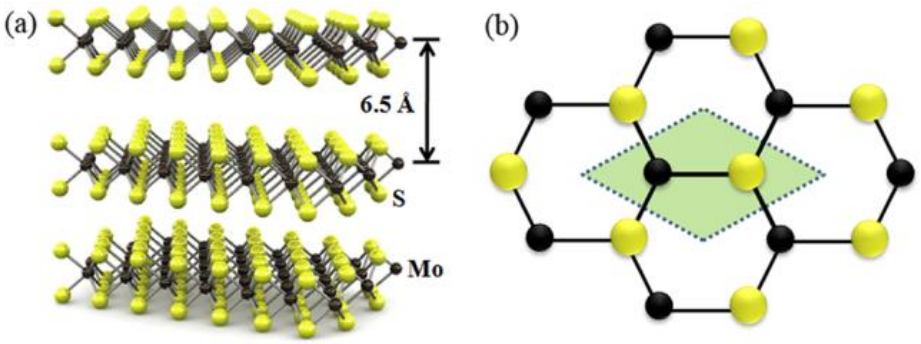

Figure 1.3 Example of a layered TMD structure. (a) The layered structure of a TMD with MX_2 stoichiometry, in this case MoS_2, composed of three atomic layers with Mo sandwiched between two layers of S. (b) Top view of a hexagonal lattice. Originally appeared in *Radisavljevic et al., Nature Nanotechnology*, (2011).[35]

Aside from graphene, another set of materials in the 2D materials family are transition metal dichalcogenides (TMDs). TMDs have a hexagonal lattice structure consisting of a layer of *M* atoms, a transition metal (e.g. W, Mo), sandwiched between *X* atoms, a chalcogen (e.g. S, Se, Te), leading to a MX_2 stoichiometry as shown in ***Figure 1.3***. TMD materials are layered structures with covalent bonding in the in-plane direction and relatively weak van der Waals (vdW) interactions in the out-of-plane directions which allows for relatively easy synthesis of few-layer TMDs through mechanical exfoliation. There is a significant amount of TMDs that exist in the MX_2 form. ***Figure 1.4*** illustrates the transition metals (in purple) and chalcogens (in yellow) that can be used to form layered selenides, sulfides, or tellurides. Of the possible TMDs, group VI TMDs (e.g. MoS_2, WSe_2, $MoSe_2$, WS_2, $MoTe_2$) are the most studied and well known due to their sizeable bandgaps and stability. ***Table 1.2*** summarizes the group VI TMDs and their respective bandgaps. An interesting structural property of these TMDs is that in bulk form they have an indirect bandgap which transitions to a larger, direct bandgap in monolayer form due to quantum confinement.[28] This has led to some interesting prospects for photonic and optoelectronic applications of TMDs.[29]

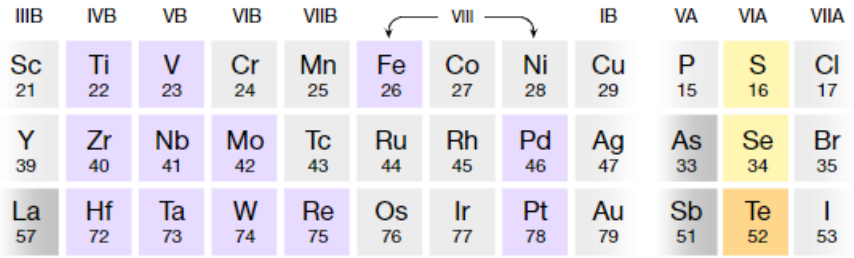

Figure 1.4 Transition metals and chalcogens used to form TMDs. Metals and chalcogens are highlighted in purple and red, respectively. Originally appeared in *Zhou et al., Nature,* (2018).[36]

Material	E_g in bulk (eV)	E_g in monolayer (eV)
MoS_2	1.2 (I)[37]	1.8 (D)[38]
$MoSe_2$	1.1 (I)[39]	1.5 (D)[39]
WS_2	1.3 (I)[40]	2.1 (D)[40]
WSe_2	1.2 (I)[41]	1.7 (D)[41]
$MoTe_2$	1.0 (I)[42]	1.1 (D)[42]

Table 1.2 Bandgaps of bulk and monolayer group VI TMD semiconductors. In parenthesis the "I" or "D" indicates whether the bandgap is indirect or direct, respectively.

1.3 Challenges in Two-Dimensional Electronics

Within the group VI TMDs, the two most widely studied are molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2). MoS_2 consists of molybdenum (Mo) sandwiched between sulfur (S) atoms with an indirect bulk bandgap of 1.2 eV that transitions to a direct bandgap of 1.8 eV in monolayer form. WSe_2 consists of tungsten (W) sandwiched between selenium (Se) atoms with a similar band structure to MoS_2 in bulk form that transitions to a direct bandgap of 1.7 eV in monolayer form. Despite the large amount of research on these materials, the inability to form ohmic contacts with most commonly used contact metals is a major impediment to further the understanding of these materials and their potential applications.

Metal-semiconductor contacts depend on several factors determined by the properties of the materials involved. When a metal with work function Φ_M is brought into contact with a semiconductor having electron affinity χ, charge transfer occurs between

them until the Fermi levels align at equilibrium (see ***Figure 1.5 b***). In the case shown in ***Figure 1.5***, when $\Phi_M > \chi$, the semiconductor Fermi level is initially above the Fermi level of the Fermi level of the metal before they are brought into contact with each other. To align the Fermi levels of them, the potential of the semiconductor must be raised relative to that of the metal. A depletion region forms near the junction and the positive charge due to uncompensated donors in the depletion region matching the negative charge on the metal, bending the energy bands of the semiconductor upwards. Once equilibrium is reached, a contact barrier prevents the flow of electrons from the conduction band of the semiconductor into the metal. Then, the potential barrier height Φ_B, known as the Schottky Barrier (SB), to be overcome for injection from the metal to the semiconductor channel depends on the difference between the metal work function and the electron affinity of the semiconductor ($\Phi_B = \Phi_M - \chi$). The formation of SB is inherent to all metal-semiconductor contacts and if not dealt with, severely limits current injection into the channel.

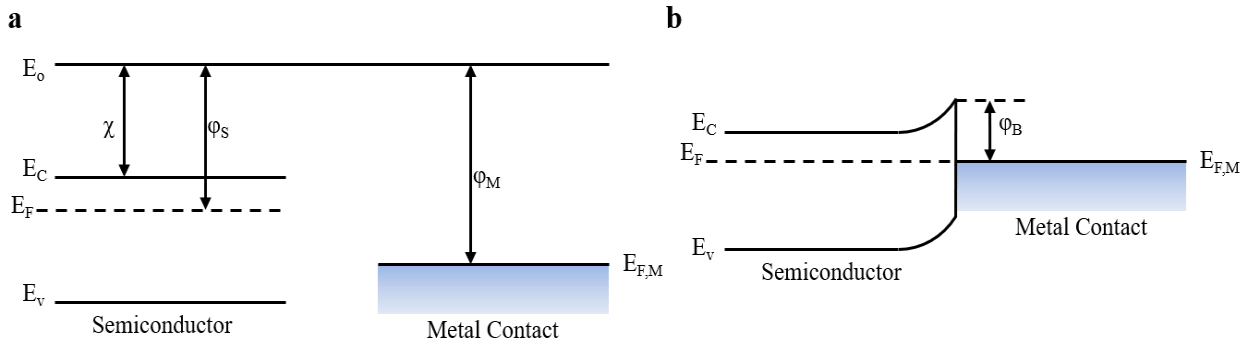

Figure 1.5 Energy band diagram for metal-semiconductor (n-type) contacts before and after being brought into contact. **(a)** In this case the metal work function Φ_M is less than the semiconductor work function Φ_S. The values of the electron affinity χ, Φ_M, and Φ_S are measured from the vacuum level E_o, the minimum energy needed to release an electron from the material. **(b)** The flat band diagram of metal-semiconductor contacts under equilibrium conditions, where the difference between the metal work function Φ_M and the electron affinity of the semiconductor χ yields the Schottky barrier height Φ_B of the contacts.

In theory, the SB can be reduced by choosing a metal work function with a value similar to the electron affinity of the channel material. Accordingly, the SB height then should follow the Schottky-Mott model, such that[43, 44]

$$\Phi_B = \Phi_M - \chi. \qquad (\mathbf{1.8})$$

However, this is an ideal case and, in reality, metal-semiconductor contacts deviate significantly from this relation.[45] In reality, choosing materials whose properties follow the Schottky-Mott model has little effect on the resulting barrier height. When a semiconductor is brought into contact with a metal, the semiconductor crystal terminates at the interface. The surface of the semiconductor contains some interface states which can result from intrinsic defects in the crystal or fabrication induced defects leading to charges at the metal-semiconductor interface. Additionally, the metal-semiconductor contact is rarely abrupt. Or in other words, the metal wave function spills into the semiconductor resulting in metal-induced gap states (MIGS).[46] These effects combine to pin the Fermi level of the semiconductor to some position within the bandgap in a phenomenon known as Fermi level pinning (FLP). The strength of FLP can be quantified by the interface parameter pinning factor *S*

$$S = \left|\frac{d\Phi_B}{d\Phi_M}\right|. \qquad (\mathbf{1.9})$$

If *S = 1*, then the Schottky-Mott model (***equation 1.8***) is followed and if *S = 0*, then this indicates very strong pinning.[47] For example, the pinning factors *S* in conventional semiconductor materials, like Si, GaAs, and Ge are known to be 0.3, 0.1, and 0.05, respectively, indicating strong pinning effects.[46, 48] While FLP generally adversely affects the metal-semiconductor junction resulting in larger than expected barrier heights, in conventional semiconductor devices it can be mitigated with heavily doped contact

regions. However, absent this ability in TMD materials, FLP is a major factor in forming contacts.

Several studies have been performed to determine the extent to which FLP plays a role in contacts to TMDs. For example, using a contact like scandium (Sc) whose work function is 3.5 eV should result in a significantly smaller SB height than using a higher work function metal as a contact like titanium (Ti) whose work function is 4.3 eV. However, this is not the case and there is a significant deviation from the Schottky-Mott model, resulting in pinning factor for MoS_2 of S ~ 0.1.[49] ***Figure 1.6*** illustrates the FLP effect in MoS_2 and WSe_2. Choosing metal work function values near the conduction band edge (i.e. electron affinity) of MoS_2 should decrease the barrier height, and likewise, choosing work function values near the valence band edge should increase the barrier height. However, as the figure shows, varying the metal work function has little effect on the tunability of the MoS_2 Fermi level. Therefore, the inevitable formation of a barrier in TMDs with most commonly used metals and the inability to mitigate this barrier with conventional semiconductor doping techniques is amplified by the strong FLP effects present. To appropriately assess the applicability of TMDs for applications and further investigate their intrinsic transport properties contact strategies that can overcome these challenges must developed.

Traditionally, in silicon devices the SB is dealt with by heavily doping the drain/source contact regions in a process known as ion implantation.[3, 50, 51] By heavily doping the contact regions, the depletion width that forms is significantly thinned so that carriers have a high probability of tunneling through the barrier. In this method, the height of the SB becomes relatively insignificant given sufficient doping concentrations. Extending this

method to TMD devices would make integration rather seamless. However, performing ion implantation doping in 2D semiconductors has proven to be impossible due to their significantly reduced thickness.[52, 53]

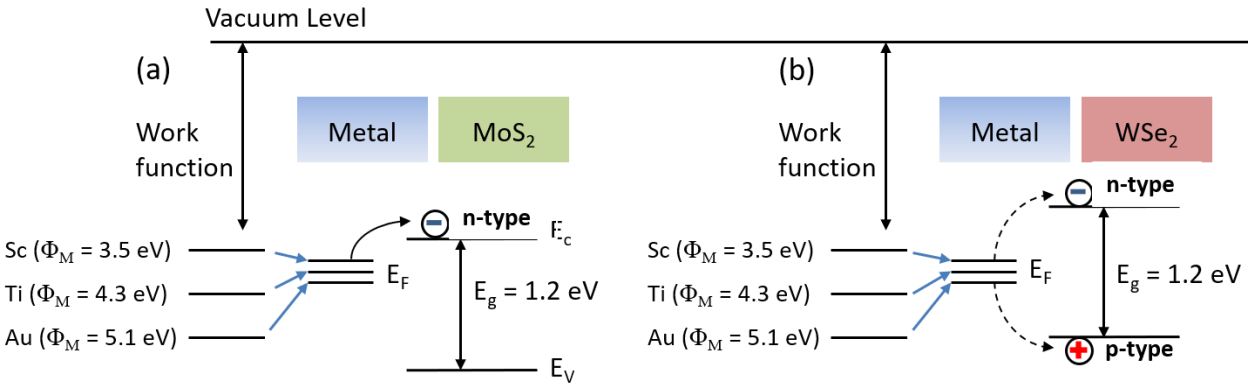

Figure 1.6 Fermi level pinning effects in **(a)** MoS_2 and **(b)** WSe_2.

1.4 Contact Approaches in Two-Dimensional Electronics

The issue of formation SB at the metal-TMD interface coupled with the strong FLP is compounded by the inability to heavily dope the drain/source regions. Conventional semiconductor doping approaches are not viable and thus new and novel approaches must be applied to make suitable contacts to TMD devices. Over the years, many approaches to making contacts have been developed. Roughly, they can be sorted into three categories: phase-engineering, chemical doping mechanisms, and interlayer contacts.

1.4.1 Phase Engineering

TMD layers can have several different phases. Semiconducting TMDs exist in the thermally stable 2H (trigonal prismatic) phase.[54] The 2H is typical in TMDs and results in the *X-M-X* (*X* = chalcogen, *M* = transition metal) stacking sequence. TMDs can also exist in a metallic 1T (octahedral) phase, which can be induced from the 2H phase.[55] Exploiting these phases, it is then possible to engineer ohmic contacts. ***Figure 1.7*** illustrates this

contact strategy, where the MoS_2 material underneath the contact metal is transformed from 2H-MoS_2 to 1T-MoS_2 using *n*-butyl lithium.[56, 57] This creates an atomically sharp phase boundary at the 1T/2H interface which results in a negligible barrier yielding drastically reduced contact resistances down to 0.2 kΩ μm.[56, 57] It is worth noting that this extremely low contact resistance is underestimated. The method by which this value was extracted is known as the transfer length measurement (TLM; for more see ***chapter 3.5***). The TLM consists of plotting the total device resistance as a function of channel length, the contact resistance is then half the *y*-intercept of the linear fit. However, it is important that the total resistance of the smallest channel length is not more than a few orders of magnitude larger than the contact resistance, otherwise the total resistance will be dominated by the channel resistance rather than the contact resistance.[58] However, in *Kappera et al.* the total resistance at the smallest channel length is nearly three orders of magnitude larger than the reported contact resistance, introducing a large amount of error.[56] Furthermore, phase engineering is difficult to reliably control, and is not thermally stable at the necessary temperature ranges for CMOS processing.

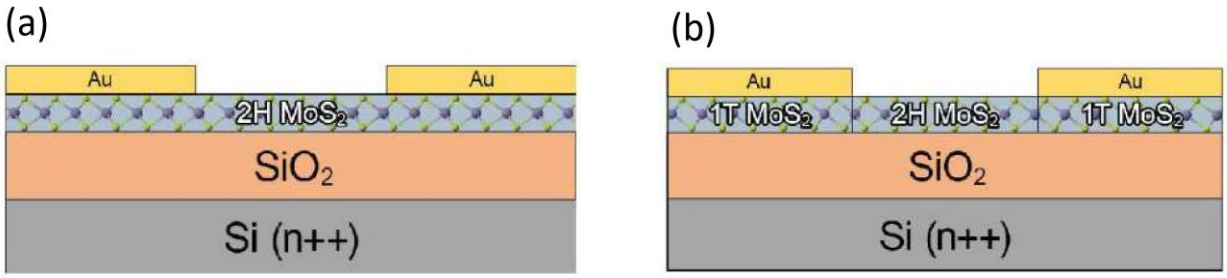

Figure 1.7 Phase-engineered MoS_2 FET. FET with Au contacts deposited on **(a)** semiconducting 2H-phase MoS_2 and **(b)** metallic 1T-phase MoS_2. Originally appeared in *Kappera et al., APL Materials,* (2014).[57]

1.4.2 Chemical Doping

Another contact engineering method to reduce the contact barrier is to use chemical methods to achieve heavy doping profiles. Chemical dopants can effectively

reduce the contact barrier at the metal-TMD interface, relying on surface charge transfer doping and the accumulation of electrons (or holes) in the channel material. These methods include doping MoS_2 via potassium vapor exposure, chloride molecular doping (***Figure 1.8 a***), and benzyl viologen (***Figure 1.8 b***) resulting in large drive currents, and reduced contact resistances.[59-62] However, these chemistry-based doping methods are difficult to control and prevent doping the entire channel material and, even still, this is not wholly effective, lacking chemical and thermal stability. Similarly, using a ionic liquid (***Figure 1.8 c***) to achieve a large double-layer capacitance to shift the Fermi level of the channel and achieve low-resistance contacts with large current on-off ratios with ambipolar transport characteristics has been achieved.[63] Yet this method is not practical for long-term applications as the use ionic liquid in full-scale commercial ICs is not a realistic option.

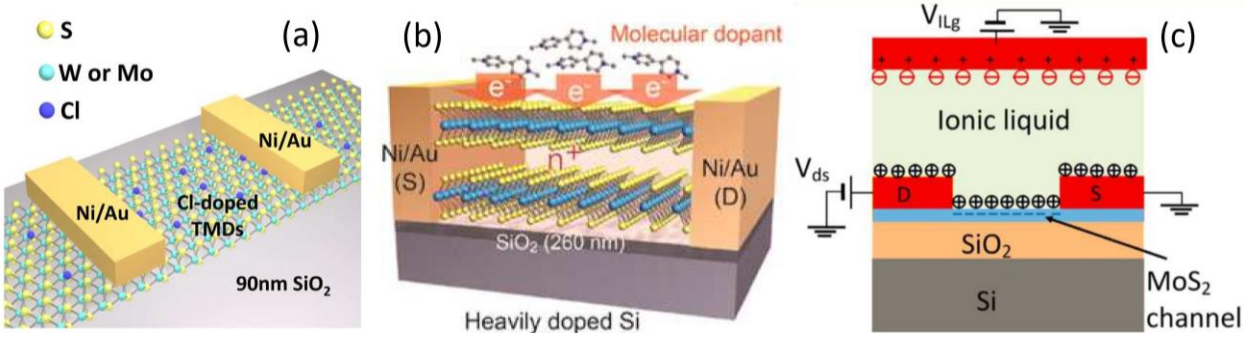

Figure 1.8 Chemical doping methods to MoS_2 FETs. **(a)** Schematic diagram of Cl-doped MoS_2 FETs using Ni/Au contacts. Originally appeared in *Yang et al., Nano Letters*, (2014).[60] **(b)** Diagram of MoS_2 FET with Ni/Au contacts using benzyl viologen doping. Originally appeared in *Kiriya et al., Journal of the American Chemical Society,* (2014).[62] **(c)** Illustration and working principle of a MoS_2 FET using an ionic liquid gate.Originally appeared in *Perera et al., ACS Nano,* (2013).[63]

1.4.3 Insulating Interlayer Contacts

Thus far the contact engineering strategies discussed have primarily focused on trying to mimic the effects of ion implantation techniques and achieving large doping

profiles at the contact interface to sufficiently thin the barrier to allow carrier to tunnel through. However, another approach is to reduce or completely remove the FLP effect all together. Essentially this relies on attenuating the MIGS by inserting some insulating interlayer material between the channel material and the contact metal, reducing the density of MIGS interaction with the channel Fermi level. To this end, ultrathin insulating materials such as metal oxides like Ta_2O_5 (***Figure 1.9 a***), TiO_2 (***Figure 1.9 b***), and MgO (***Figure 1.9 c***) have been used as interlayer materials inserted between the channel and contact metal.[64-66] The relative band offsets, the difference between the insulating interlayer electron affinity and that of the semiconductor channel, at the Ta_2O_5/MoS_2 and TiO_2/MoS_2 interfaces make Ta_2O_5 and TiO_2 ideal for minimizing the series tunneling resistance at the contact interface. However, since semiconducting TMDs are layered and, therefore lack out-of-plane covalent bonds, depositing uniform ultrathin layers of metal oxides on them is challenging because chemical groups such as hydroxyl radical are usually required to form conformal, uniform interface layers.[67-70]

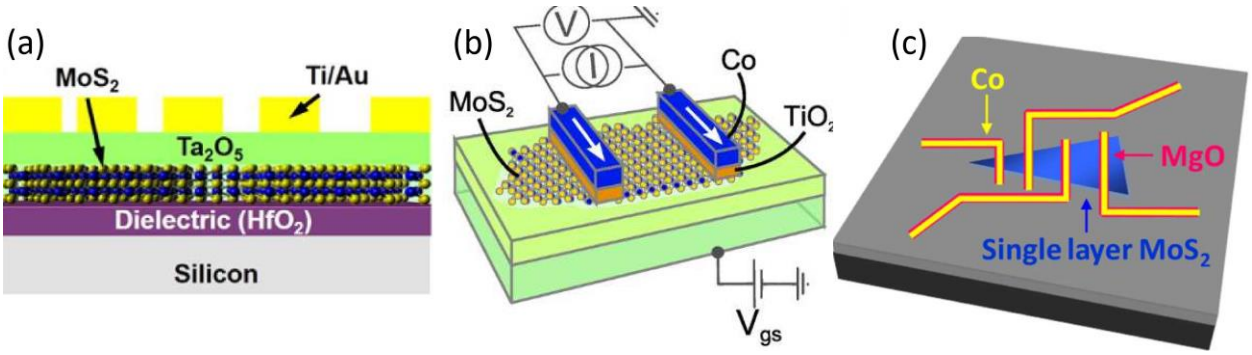

Figure 1.9 Insulating interlayer contacts to MoS_2 FETs using metal oxides. **(a)** Schematic diagram of a MoS_2 FET using Ta_2O_5 inserted between the Ti/Au contacts and the MoS_2 channel. Originally appeared in *Lee et al., Nano Letters,* (2015).[64] **(b)** Diagram of a MoS_2 FET using TiO_2 interlayer contacts between MoS_2 and Co contacts. Originally appeared in *Dankert et al., ACS Nano,* (2014).[65] **(c)** Illustration of a MoS_2 using MgO between the Co contacts and MoS_2 channel. Originally appeared in *Chen et al., Nano Letters,* (2013).[66]

The challenge of depositing uniform and ultrathin metal oxide layers on semiconducting TMD interfaces poses a problem for continued growth of this engineering strategy using traditional oxide formation processes. On the other hand, 2D vdW materials would make better candidates as interlayer materials as they are capable of forming atomically clean and uniform interfaces without the constraints of lattice matching or surface functionalization. Ultrathin hexagonal boron nitride (hBN) has been demonstrated as an insulating interlayer contact material to MoS_2 (see ***Figure 1.10***) to effectively reduce the SB height and the contact resistance.[71] However, since hBN has a relatively small electron affinity relative to MoS_2 there is a significant band offset between the two. This leads to a high tunneling barrier in series with the SB because the resistance of the tunneling barrier exponentially increases with the product of the barrier with and the square root of the barrier height.[72] Minimizing this tunneling barrier while simultaneously achieving a small SB height is key to realizing ohmic contacts with interlayers.

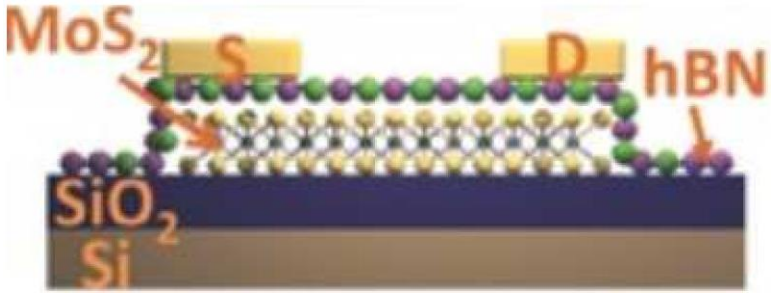

Figure 1.10 hBN interlayer contacts to MoS_2 FET. Schematic of a MoS_2 FET with hBN interlayers inserted between the contact metal and the MoS_2 channel. Originally appeared in *Wang et al., Advanced Materials,* (2016).[71]

1.4.4 Semiconducting Interlayer Contacts

Interlayer contacts present an opportunity to achieve high-quality contacts, provided the band offset is minimized and the fabrication process can yield conformal,

intimate contact with the channel material. Some metal oxides have a favorable band alignment to MoS_2, yet they cannot be deposited effectively. Conversely, hBN can be placed atop MoS_2 with atomic conformity and yield an ultra-clean interface, but the unfavorable band alignment between hBN and MoS_2 inhibits performance. Logically, if the strengths of each interlayer contact strategy could be utilized, favorable band alignment combined with an atomically thin and uniform interface, superior contacts can be formed. There are many semiconducting TMDs whose band offsets relative to each are quite small. Additionally, the formation of hetero structures by stacking semiconducting interlayers ensures atomically clean interfaces. Using semiconducting interlayers as an interlayer material to semiconducting channel materials can simultaneously minimize the tunnel barrier through favorable band alignments and high-quality interfaces through vdW bonding.

1.5 Scope of the Dissertation

This dissertation focuses on the contact properties of MoS_2, specifically how the addition of a 2D semiconducting interlayer affects the contacts. ***Chapter 2*** introduces the fabrication techniques developed and used in this research as well as the primary characterization methods. To study the impact of inserting 2D semiconductors at the contact interface, between the MoS_2 channel and the contact metal, MoS_2 FETs were fabricated with several different interlayer materials as well thicknesses. The resulting impact on the contact barrier height and how the contact resistance, resistivity, and transfer lengths change with interlayer material is presented in ***chapter 3***. Ultimately, the insertion of an interlayer at the contact interface improves the contact quality substantially. ***Chapter 4*** discusses the details of the performance increase and how various interlayer

materials affect it. Finally, in ***chapter 5*** we briefly discuss the prospects for future applications of this contact method to other materials as well as its viability for use in large-scale fabrication.

Chapter 2 DEVICE FABRICATION AND CHARACTERIZATION

This chapter focuses on the primary techniques and methods used to fabricate 2D FETs as well some of the methods used to characterize them. Fabricating 2D FETs requires a combination of standard semiconductor processing methods, including lithography, metal deposition, and electrical characterization, and 2D material specific techniques, such as mechanical exfoliation, vdW transfer, and nano-squeegeeing. This section gives an overview of both, with a heavier focus on the 2D material techniques.

2.1 Mechanical Exfoliation of 2D Materials and TMDs

Mechanical exfoliation of layered materials has been the primary way that atomically thin materials have been synthesized for device applications in a research setting. The popularity of this method started with the isolation of graphene.[73] Mechanical exfoliation involves continuously cleaving a bulk crystal into increasingly thinner flakes until the flakes are deemed sufficiently thin. The primary figures of merit in this process are sample size or total area, thickness, and cleanliness. The area of samples obtained is important, as many of the subsequent processing steps have relatively limited resolution (e.g. materials transfer) and material sizes on the order of tens of micrometers make these processes easier. As discussed in ***chapter 1***, many 2D materials exhibit interesting properties at the atomic thickness scale and also present unique opportunities to overcome challenges related to scaling in traditional semiconductor materials. Due to this, achieving material thicknesses in few-layer and monolayer form is essential for furthering the study of 2D materials. The cleanliness of the exfoliated samples is most important, if the interface quality is not residue free then the performance of subsequently fabricated

devices will be severely affected by this. Initially, the exfoliation methods developed for 2D materials made use of “Scotch tape.” The use of non-specialized tape for this task led to the introduction of large amounts of residue which ultimately hampered the device quality. In subsequent years, methods were developed to minimize the residue remaining on the surface and yield larger area flakes.[74] Further still, we have developed methods to exfoliate samples that are of large area, with atomic thickness, and are ultraclean, with consistency.

2.1.1 Substrate Preparation and Cleaning

2D FETs are fabricated on substrate. In this case, a substrate of *p*-doped silicon with a silicon oxide (SiO_2) layer. To assist with sample identification and subsequent processing steps, like alignment during electron beam lithography (EBL), alignment marks are needed on the substrate. These alignment marks are made on a 4-inch wafer, using a standard photolithography process, the subsequent substrate pieces are then cut from the wafer.

Figure *2.1* outlines the processing steps used to make alignment marks. The wafer must be free of contaminants and moisture, both of which can cause processing problems in the later steps of lithography processing. Si/SiO_2 wafers have polar surfaces and thus are likely to absorb moisture. To remove moisture that may have been absorbed by the wafer, it is dehydrated on a heating element. Hexamethyldisilazane (HDMS) is an adhesion promoter that is applied to the wafer surface after dehydrating the surface. HDMS makes the surface hydrophobic, ensuring that the photoresist (PR) that is subsequently applied, adheres well to the wafer. Once the PR is spun on through a spin-

coating procedure, a soft-bake is performed. Soft baking is done for a number of reasons, it drives away the solvents contained in the PR, it further improves the adhesion of the PR to the wafer, and also anneals the stresses introduced during the spin-coating procedure. Once the wafer has been prepped through PR application and soft baking, it undergoes a UV (ultraviolet) light exposure which forms a pattern on the wafer. This is accomplished by using a mask which defines the areas on the wafer surface where the pattern defined by the mask will be transferred. When using a positive PR, the areas exposed by the UV light become more soluble. After the wafer is exposed, a post-exposure bake (PEB) is performed to assist with the chemical reactions taking place in the PR due to exposure. The PEB is then followed by pattern development. To develop the pattern, the wafer is immersed in a solvent which removes the more soluble areas (i.e. the areas exposed). While the development step removes a majority of the exposed areas, a thin layer of resist still remains on the surface. To remove this thin film of PR an oxygen plasma, or descum process, is performed to remove the remaining layers. Metal (typically Ti/Au) is then deposited in the exposed area through an evaporation process, coating the entire wafer. The wafer is then cut into ~ 2 cm x 2 cm squares and submerged

in acetone to liftoff the PR and metal from the surface. This results in a substrate with alignments necessary for further processing.

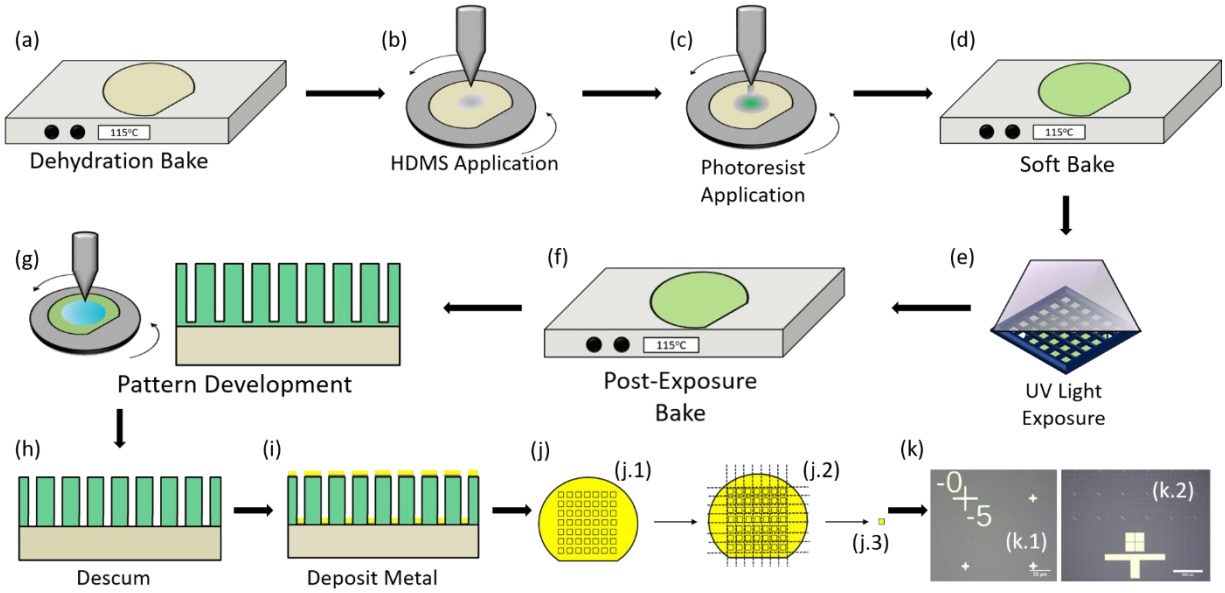

Figure 2.1 Workflow diagram of photolithography process for making alignment marks. The wafer is first prepped using a **(a)** dehydration bake to remove any absorbed moisture and **(b)** HDMS is applied to act as an adhesion layer between the photoresist (PR) and the surface of the wafer. **(c)** PR is spun on and (d) soft baked to remove any solvents in the resist. Using a contact aligner, the wafer is **(e)** exposed to UV light then **(f)** baked to assist the chemical reactions in the resist. Next, the exposed pattern is **(g)** developed. This is followed by a **(h)** descum, where low-power oxygen plasma is used to etch away any remaining PR residue on the surface of the wafer. **(i)** Metal is deposited in the exposed areas. **(j)** The result is a 4-inch wafer with many different substrates of **(j.1)** ~ 2 cm x 2 cm, which is then **(j.2)** cut into smaller pieces resulting in many **(j.3)** single substrates. **(k)** Each individual substrate is then lifted off in acetone and sonicated revealing a **(k.1)** coordinate system for use during alignment in electron beam lithography and a **(k.2)** large alignment mark for orientation during this process.

In exfoliation it is essential that the substrate surface is free of contaminants, such as moisture and other organic materials as this ensures that the exfoliated crystals can adhere sufficiently to the surface of the substrate. To achieve this, an oxygen plasma cleaning step is performed on the substrates prior to application of the exfoliated tape. In this step the contaminants and impurities are removed from the surface. Oxygen plasma contains atoms, molecules, ions, electrons and free radicals all of which interact with the

surface of the substrate as shown in **Figure *2.2***. Together, these work to remove any contaminants and organic materials, leaving an ultraclean substrate surface.

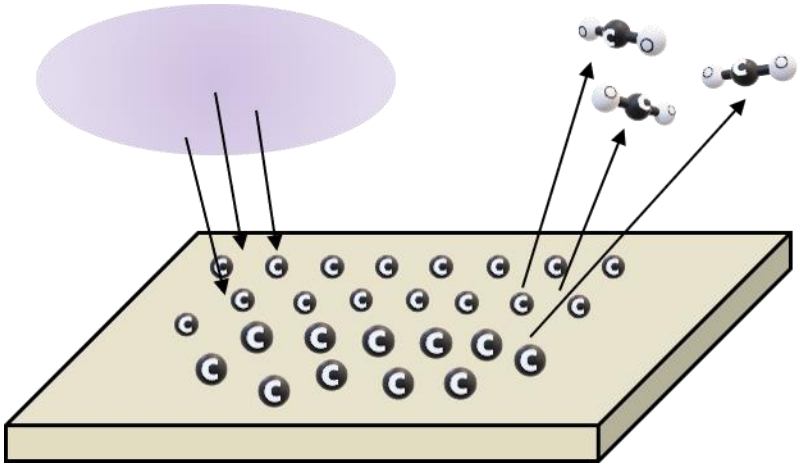

Figure 2.2 Oxygen plasma cleaning of SiO_2 substrate.

2.1.2 Mechanical Exfoliation

Once the substrates have been fabricated and properly cleaned through oxygen plasma, the tape used for mechanical exfoliation of ultrathin 2D flakes is prepared. A special residue reducing tape is used to minimize the transfer of contaminants, ensuring that the cleanliness of the resulting flakes will be better than those made from "Scotch tape." The tape is cut into two equal parts as shown in **Figure *2.3(a)*** and the protective backing removed from each (**Figure *2.3 b***). The bulk crystal of the material to be exfoliated is placed in the top corner of one of the pieces of tape (**Figure *2.3 c***) and the second piece of tape is placed over top the crystal and pressed (**Figure *2.3 d***). This process is repeated until each of the pieces of tape are covered with thin flakes as shown in **Figure *2.3(e)***. By repeatedly cleaving the bulk crystal from each the tape the samples are continuously thinned before they are transferred to the substrate surface. To maximize the chances of creating ultrathin samples with large area, the density of

exfoliated flakes is important. The larger the density of exfoliated crystals, the higher the probability that these ideal flakes will be transferred to the substrate.

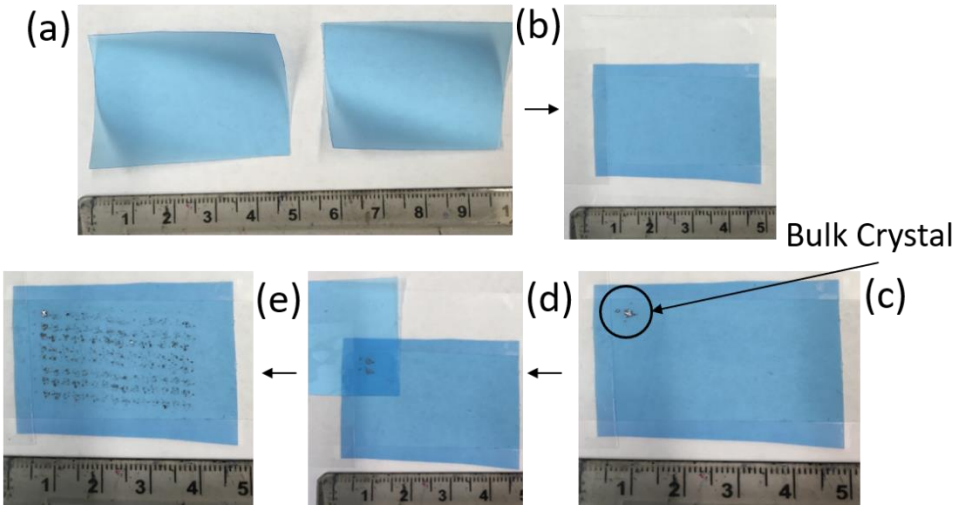

Figure 2.3 Exfoliation using ultraclean tape. **(a)** Tape is cut into two squares. **(b)** The backing is peeled back and **(c)** the bulk crystal is placed in the top corner. **(d)** The second piece of tape is placed over top of the crystal and **(e)** peeled back repeatedly thinning the crystal.

Now that the crystal has been exfoliated on tape and the substrate has been cleaned through a oxygen plasma process, the tape is placed on the substrate (**Figure *2.4 a***). The tape is then pressed continuously for approximately five minutes (**Figure *2.4 b***). Pressing the tape functions to remove any air that is trapped between the substrate and tape, promoting adhesion between the 2D flakes and substrate. Traditionally, the next step in the exfoliation process would be to remove the tape from the substrate. However, this usually leads in a low yield of high-quality flakes. To facilitate more consistent realization of high-quality flakes a heating step has been introduced before tape removal.[74] In this heating step the substrate was placed facing up (i.e. tape away from the heating element). This method, while offering some improvements from those previously performed, does not reach the full potential of heating. Instead, we have developed, and introduced some innovations to this method which greatly increase the

yield. After pressing, the tape/substrate is placed face down on the heating element (i.e. tape towards the heating element) as shown in **Figure *2.4(c, d)***. This modification serves to remove any remaining air pockets between the tape and substrate by allowing the tape and its backing conform around the substrate, squeezing it tightly, creating a seal. This guarantees maximum intimate contact between the crystals on the tape and the substrate. In addition, previous methodologies posited that it was best to remove the tape from the heat and peel it in a slow, steady motion. However, this still leaves some residue on the surface and does not provide maximal yield. To avoid such issues, we do not allow the substrate/tape to cool before removing the tape. Instead, while still in contact with the heating element, the tape is removed from the substrate. Since the tape is still warm and partially melted, the adhesion glue on tape is melted enough so that it no longer adheres strongly to the substrate, while the flakes on the tape now adhere more strongly to the substrate through vdW bonding leaving residue free surfaces. **Figure *2.5(a-c)*** show examples of exfoliated 2D flakes resulting from this innovative exfoliation method. Clearly, it yields large-area samples that are atomically thin with a residue-free surface.

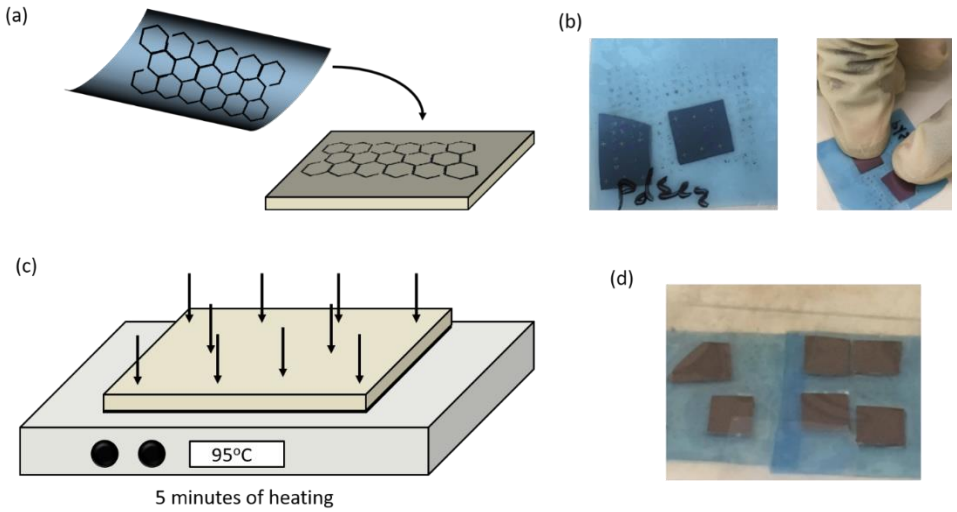

Figure 2.4 Heating exfoliation of 2D materials. **(a)** The exfoliated tape is placed on a clean SiO_2 substrate and **(b)** pressed continuously to remove and air traps. **(c)** The

tape/substrate is placed crystal side down on the heating element for 5 minutes at 95°C, **(d)** creating a seal around the substrate and the tape is removed from the substrate while still in contact with the heating element.

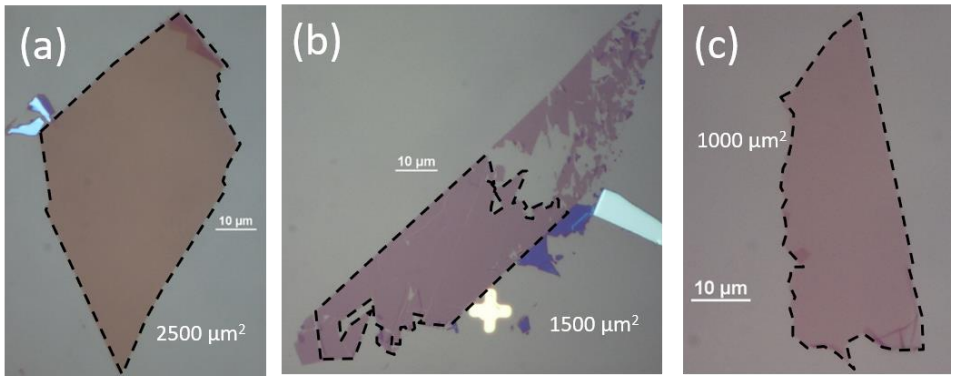

Figure 2.5 Examples of large-area exfoliated **(a)** WSe_2, **(b)** MoS_2, and **(c)** $MoSe_2$ flakes on SiO_2 substrates.

2.2 van der Waals Assembly of 2D Materials and TMDs

In fabricating devices with 2D materials and TMDs, an important process is the ability to reliably pickup and transfer exfoliated materials. Using this method, exfoliated materials can be aligned, stacked, and transferred onto one another with a high degree of precision and cleanliness.[22, 75, 76] To accomplish this, we have used and improved upon a dry pickup method. This method removes some of the issues related to other materials transfer and growth methods, like CVD or other PMMA based methods which can introduce some residue.[75, 77]

2.2.1 Dry Pickup Method

The dry pickup method is facilitated by first placing a thin film of polycarbonate (PC) on a glass microscope slide using a polydimethylsiloxane (PDMS) stamp as a backing. The PC film is prepared by, first combining 3.0 g of PC with 0.18 mL of chloroform (~16:1 ratio) and placing it on a shaker for approximately 30 minutes to allow

the PC and chloroform to combine. After this time the PC will be fully mixed with chloroform, creating a viscous solution that can be spread on the PDMS stamp that has been cut into small square (~ 0.5 x 0.5 cm). The PC is placed on the PDMS stamp using a micropipette so that a small amount (~ 20 µL) is spread on the stamp and flattened. The PC is then allowed to dry on the PDMS stamp for 5 minutes.

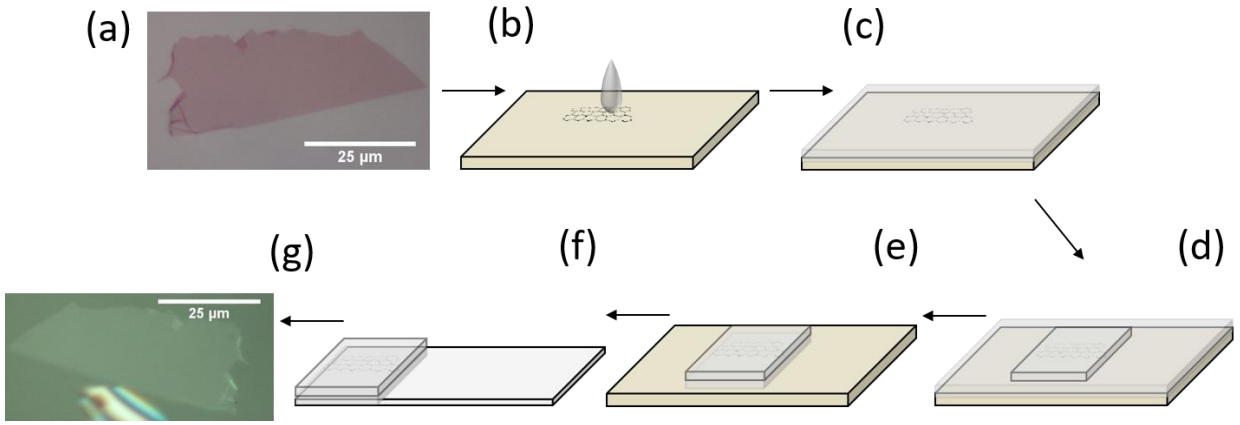

Figure 2.6 Steps involved in picking up a 2D flake from SiO_2 substrate. **(a)** The sample desired for pickup is **(b)** covered with PC film and **(c)** flattened over the sample. **(d)** A PDMS is cut and placed over the PC film and sample. **(e)** The excess PC film and PDMS is cut away and the PDMS/PC/sample is **(f)** picked up from the substrate and **(g)** put on a glass slide.

To pickup and transfer samples, a modified probe station setup is used. ***Figure 2.7(a)*** shows an illustration of this setup. It consists of an optical microscope, micromanipulator, and heated sample holder. Once the PC has dried, and the sample targeted for pickup is identified, the substrate containing the target sample is placed on the stage of the transfer setup as pictured in ***Figure 2.7(a.1)***. The PC/PDMS stamp that is on the microscope slide is placed in the micromanipulator sample holder. The target sample is found using the optical microscope and then positioned correctly beneath the PC/PDMS stamp. Micromanipulator is used to approach the PC/PDMS stamp close to the substrate. Just before the approach is complete, the sample holder is heated to 100^{o}C. Then the manipulator is used to further approach the PC/PDMS stamp, bringing

it fully in contact with target sample. The heating of the sample holder serves to remove any bubbles that may be present between the sample and PC/PDMS stamp. After the approach is complete ***Figure 2.7(a.2)***, the temperature is further increased to 135^{o}C and held for two minutes. This partially melts the PC film, allowing for the film to conform around the target sample. After heating for two minutes, the manipulator is used to remove the PDMS stamp from the substrate ***Figure 2.7(a.3)***, because of the heating step the PC will remain on substrate, covering the target sample. After cooling the substrate, the PC film can be carefully removed from the substrate. The film will contain the target sample, now picked up. This process is then repeated using the same PC film to stack subsequent 2D materials. Once the last pickup and transfer is completed, the substrate with PC film still on it is placed in a chloroform bath (as shown in ***Figure 2.7 b***). The chloroform will function to dissolve the PC film but leave the transferred and stacked sample on the substrate. This pickup method, using 2D materials to subsequently pickup other materials, minimizes the probability of residue remaining on the transferred materials, leaving high-quality interfaces.

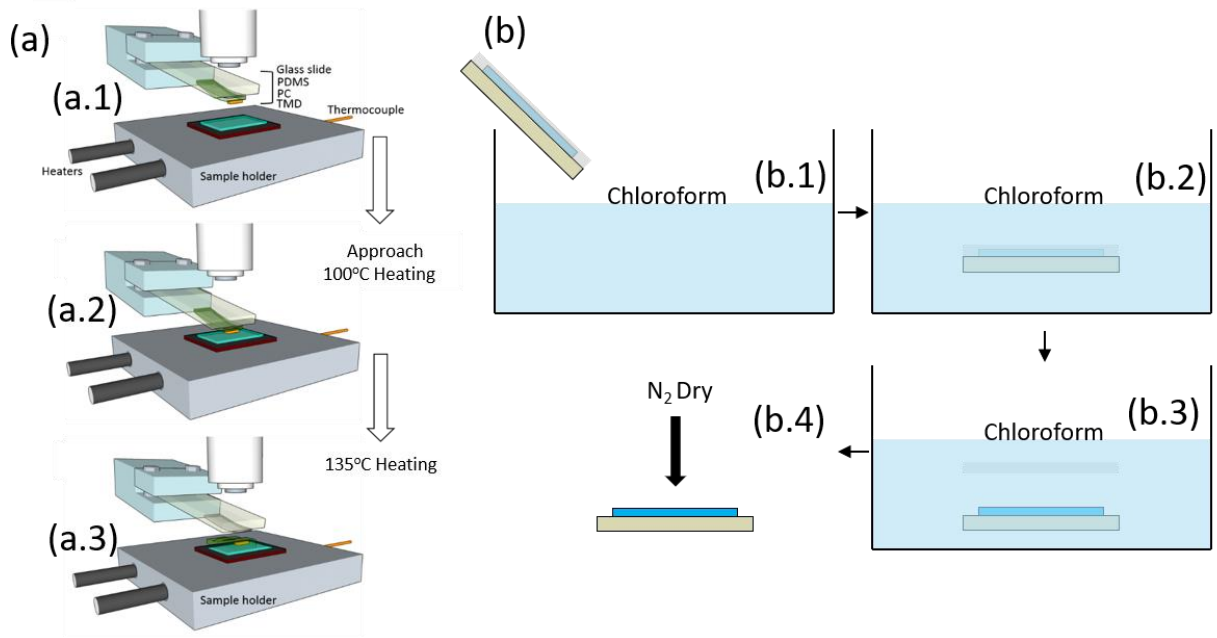

Figure 2.7 Schematic illustration of transfer steps and PC film rinse in a chloroform bath. **(a)** Diagram of transfer stage with micromanipulator, heating element, stage, and microscope. **(a.1)** The sample to be transferred is placed in the micromanipulator and approached toward the target substrate while heating at 100°C. **(a.2)** The sample is touched down on the desired target substrate and heated at 135°C for 2 minutes. **(a.3)** The manipulator is used to remove the glass slide from the target substrate, leaving the transferred sample contained in the PC film on the target. **(b)** Upon cooling, **(b.1-3)** the sample is placed in a chloroform bath, which dissolves the PC film. **(b.4)** After 10 minutes, the substrate is removed from the bath and dried with N_2.

2.3 Electron Beam Lithography

Electron beam lithography (EBL) is a useful technique for fabricating electrodes to nanoscale devices. For research purposes, it is useful because each device structure has unique requirements and, thus requires a versatile and cost-effective approach to patterning electrical contacts as opposed to the more traditional method of photolithography employed in high volume manufacturing operations. Since no hard mask is required for EBL, a unique pattern can be generated to fit each device design as opposed to constraining device size and geometry to the mask size or creating costly hard masks for each design. In our case, a scanning electron microscope (SEM) with an

EBL attachment is used as shown in **Figure *2.8***. With the use of a nanopattern generation system (NPGS), unique patterns can be designed and written using EBL.

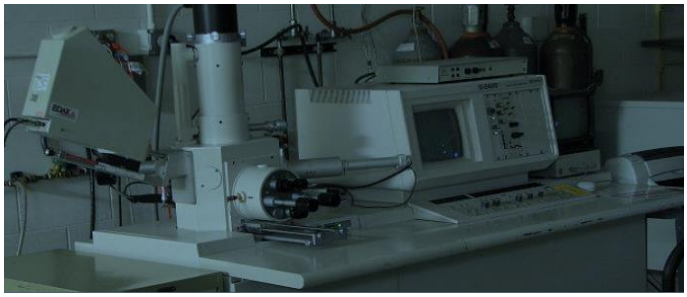

Figure 2.8 Scanning electron microscope (SEM) with electron beam attachment

Aside from greater flexibility, an EBL allows for increased resolution as compared to general photolithography. This is due to the differing mechanism employed in EBL, where a small-diameter focused beam of electrons is accelerated toward to the surface of the sample. The resolution limit in EBL is dependent on the generation source of electrons and beam diameter, rather than diffraction limits as in photolithography. **Figure *2.9*** shows a simple diagram of an EBL system which consists of an electron source that supplies the electrons, a column that focuses the beam through several lenses and apertures, a mechanical stage that allows for sample positioning, and a computer feedback system that controls the writing equipment.

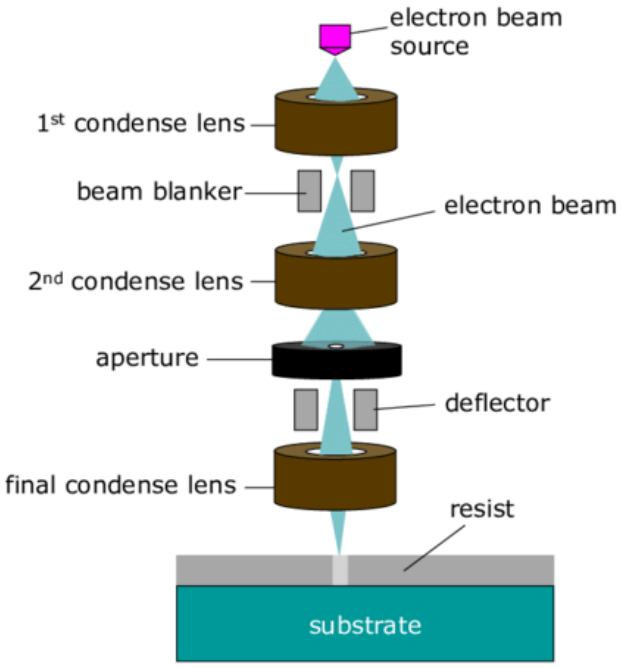

Figure 2.9 Schematic illustration of electron beam lithography (EBL) system.

The purpose of EBL is to write a pattern for the eventual formation of metal electrodes on the sample surface. To achieve this desired area is exposed by accelerating electrons toward the surface. The substrate surface is coated with resist, polymethyl methacrylate (PMMA). In later processing steps, metal will be deposited on the surface serving as the electrodes. To remove the metal a process called liftoff is used. To assist with this process, a common method of resist application for EBL is to use bi-layer resist. In this case, the bottom layer of resist that is spun on has a higher sensitivity (495K PMMA) than the top layer (950K PMMA) (**Figure *2.10 a-c***). When the electrons strike the surface, they interact with the PMMA and since the since the top layer is less sensitive than the bottom layer, the bottom layer is more exposed than the top, creating an undercut (**Figure *2.11***), essential for liftoff applications.

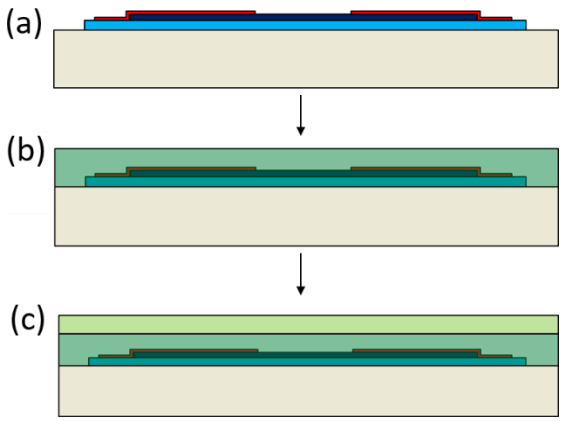

Figure 2.10 Electron beam lithography (EBL) bi-layer resist application. **(a)** The finished device is first **(b)** coated with 495K PMMA and hard baked. Then a layer of **(c)** 950K PMMA is applied, followed by another hard bake.

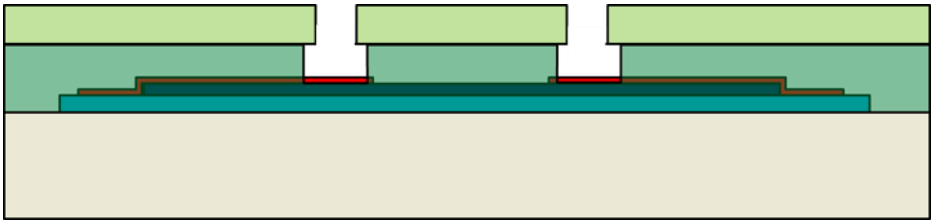

Figure 2.11 Example of bi-layer PMMA resist undercut.

Upon completion of EBL pattern writing, the pattern on the sample is developed. The development process consists of immersing the sample of a developer solution which is a mixture of methyl isobutyl ketone (MIBK)/IPA (1:3 ratio) and a small amount of methyl ethyl ketone (MEK) that acts a developer enhancement solvent. The substrate is place in this solution for 70 seconds and gently shaken during this time. After this time, the substrate is removed from the developer and briefly washed off with IPA and blown dry with N_2 gas for pattern examination. **Figure *2.12*** shows an example of a developed pattern at 10x and 100x magnifications. It is important that the EBL process is properly tuned so that the features are fine. This is achieved by correct beam and exposure conditions, and the samples surface is free of PMMA residue.

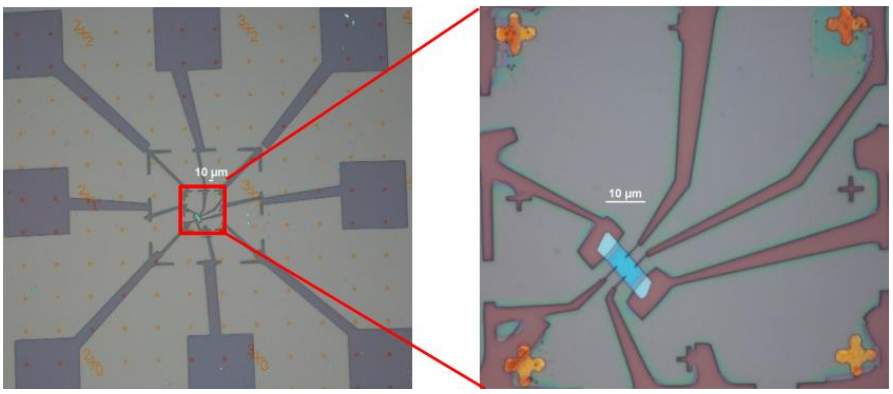

Figure 2.12 Pattern development after electron beam lithography exposure.

2.4 Metal Deposition

Once the desired pattern has been written with EBL and developed, electrical contacts are formed in exposed regions. There exist several processes to achieve the deposition of metal onto the surface of a sample, collectively known as physical vapor deposition (PVD). The two primary methods of PVD are sputter deposition and evaporation. The former involves exposing a target material, that is to be deposited, to a plasma which condenses on the substrate surface forming a thin film. However, since liftoff is the process by with excess metal and PMMA will be removed, sputtering is not ideal here. This is because sputter deposition is a highly conformal process and would lead to metal being deposited on the sidewall areas of the resist, making it difficult to remove. In evaporation, specifically electron-beam assisted evaporation, a target anode is bombarded with an electron beam from a tungsten filament. The electron, accelerated to a high energy, hit the target and melt the material into a gaseous state. The gaseous atoms then precipitate into the solid phase and coat the deposition chamber as depicted in ***Figure 2.13***.

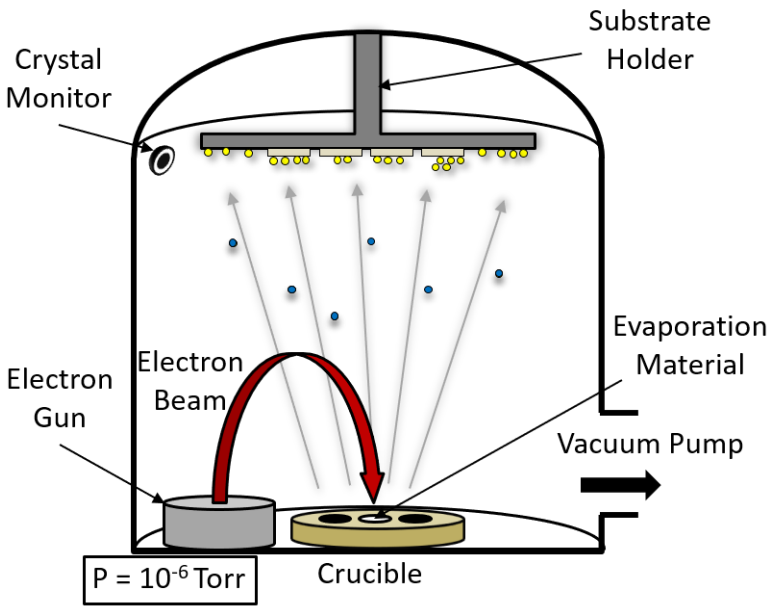

Figure 2.13 Schematic illustration electron-beam assisted evaporation chamber.

In electron beam evaporation for the purpose of liftoff there are several important parameters to be considered. First, the ratio of resist (PMMA) thickness to total evaporated metal must be relatively large, ideal greater than 5: 1 (i.e. the thickness of the metal should be at least five times that of the resist thickness). A large ratio of resist to metal ensure that there will be a significant discontinuity between the deposited metal and the top of the resist. **Figure *2.14*** illustrates the principle of large discontinuity, where the metal deposited on the surface is small compared to the total height of resist. This is also aided by having nearly perpendicular deposition angle. If the angle by which the metal particles reach the substrate relative to the vertical direction is not 90^{o}, then this will also make liftoff more difficult. When the deposition is not perpendicular the metal film will also coat some of the sidewalls of the resist and thus effect the discontinuity of metal and resist. To deposit metal for electrical contacts using electron beam evaporation we used a two-step deposition process. In the first step, a thin layer of titanium (Ti) is deposited (~ 5 – 10 nm) which acts as an adhesion layer. Ti is typically chosen as an adhesion layer

metal because when using a Si/SiO_2 substrate, the Ti bonds easily with the abundant oxygens on the surface of the substrate. Second, a layer of gold (Au) is deposited (~ 40 – 50 nm) which serves at the primary electrode material.

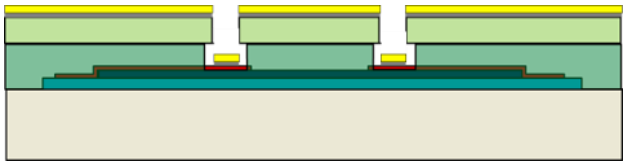

Figure 2.14 Sample after deposition of Ti/Au.

2.5 Liftoff

Once the metal for electrodes has been deposited on the sample surface, the excess metal and resist must be removed. This process is known as liftoff. In liftoff, the sample is immersed in acetone for some period of time, typically 10 – 20 minutes. In this time the undercut created during the EBL patterning functions to remove the resist and metal from the unexposed regions. Here the quality of EBL patterning and deposition are the primary factors in determining the ease of liftoff. If there has been no sidewall coating, then the liftoff will be easy, and the result will be similar to the example shown in ***Figure 2.15***.

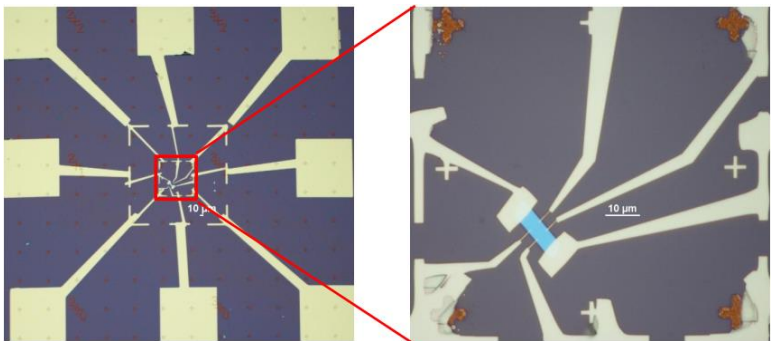

Figure 2.15 Optical image of sample after liftoff, showing 10x and 100x magnification.

2.6 Annealing

Sample annealing serves several purposes in processing. First, it is sometimes necessary to anneal fabricated samples prior to EBL processing. This is largely to due difficulty in reducing all defects that arise through vdW assembly. By annealing these devices prior to further processing, the organic matter, air traps, or other contaminants can be minimized or removed completely. Also, vdW assembly sometimes introduces stresses and strains to the transferred materials, annealing can also function to relax them. Second, as stated above, Ti is used as an adhesion layer for metal deposition. Ti reacts rather strongly with ambient conditions, and even though it is protected by the Au layer on top of it, it is still possible some oxidation may occur (e.g. Ti + O_2 → TiO_2). Annealing devices after metal deposition or after long-term exposure to ambient conditions can help remove some oxidized material that is detrimental to carrier injection into the FET.

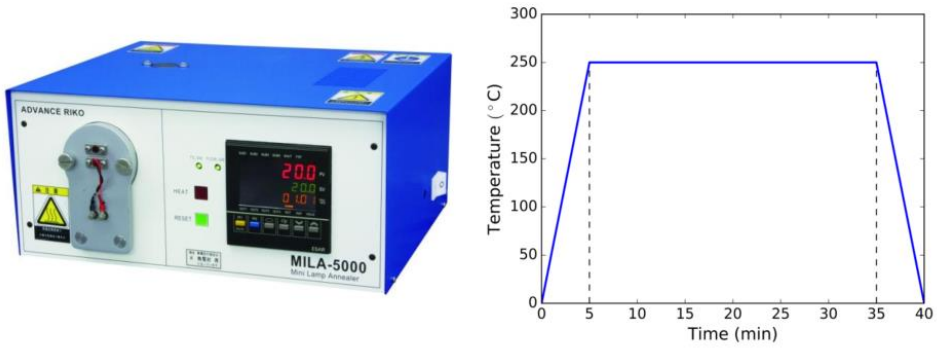

Figure 2.16 (a) Vacuum annealing setup. **(b)** Temperature program for annealing devices.

The annealing setup is shown in **Figure *2.16(a)***. Samples are placed inside and pumped down to vacuum while purging the chamber with form gas (a mixture of 10% H_2 and 90% Ar) to remove residual oxygen and water molecules from the chamber that could otherwise adversely affect the materials inside. Once under vacuum and purged, the

annealing program is set to run. **Figure *2.16(b)*** shows an example of a typical annealing program over time. In this example, the temperature is increased from room temperature to 250^{o}C over 5 minutes and then held at this temperature for 30 minutes. After the completion of the programmed annealing time, the chamber is then cooled back to room temperature and the sample is removed.

2.7 Device Characterization

Principally, the purpose of fabricating FETs is to measure their properties. This can be done through a number of means, either structural or electrical. Through these characterization techniques, information about their cleanliness, thickness, and electrical performance can be known. In this section, the primary means we have used to characterize FETs are described as well as their basic operation and meaning. This will serve as a basic foundation for discussion of the results obtained using these methods in the subsequent chapters.

2.7.1 Atomic Force Microscopy

Atomic force microscopy (AFM) can be used for a number of purposes. The primary use of AFM, however, is to characterize the surface of a material. It can be used to determine sample cleanliness through studying surface roughness and mapping the sample surface to determine its thickness. An AFM (**Figure *2.17 a***) is a scanning probe microscope equipped with a sharp tip (**Figure *2.17 b***). The tip is connected to a cantilever to scan over the sample surface. The tip is brought near the sample surface, as this occurs the tip is attracted to the sample and the cantilever is deflected toward the surface.

As the tip is brought closer to the surface, an increasingly repulsive force begins to dominate, deflecting the cantilever away from the sample. This deflection can then be monitored by a laser beam that reflects off of the cantilever. When the cantilever is deflected by any amount, the direction of the reflected beam will be registered. Using this method, the entire surface of a sample can be mapped, and the line profile of sample edges can be determined (**Figure *2.17 c***), as the thickness is of great importance in 2D FET fabrication.

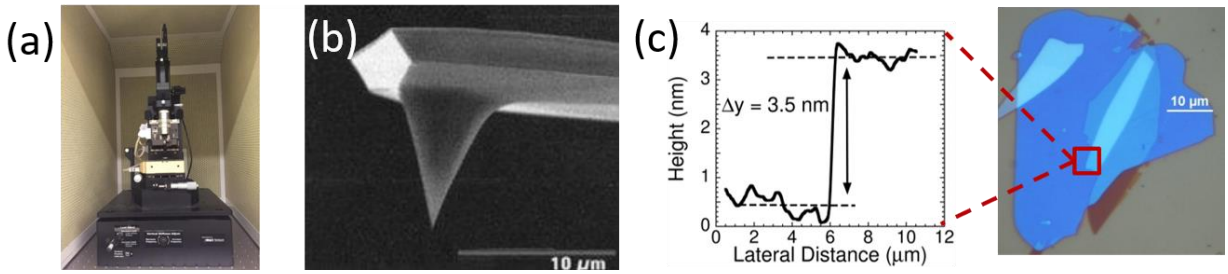

Figure 2.17 (a) Atomic force microscope (AFM) setup. **(b)** Magnified image of AFM tip. **(c)** Example line profile resulting from AFM scan on device to determine flake thicknesses.

2.7.2 Electrical Measurements

Perhaps the most important characterization method for our purposes to study device properties is electrical characterization. There exist many different measurement configurations to elucidate specific material and device parameters. In this section, only basic measurement results and properties will be discussed. To perform electrical characterization test, a Keithley 4200 SCS semiconductor parameter analyzer system is used to control the applied voltage and collect data (**Figure *2.18***).

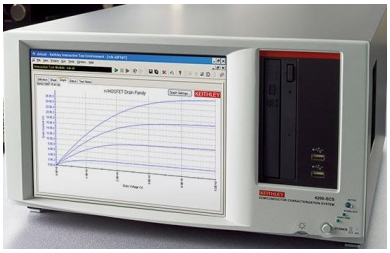

Figure 2.18 Keithley 4200 SCS semiconductor parameter analyzer system.

Simple current – voltage measurements are taken in order to study the electrical characteristics of FETs. Current – voltage measurements exist in two forms. First, drain current versus drain voltage (I_{DS} – V_{DS}), shown in **Figure *2.19(a)***. In this measurement, the drain current (I_{DS}) is measured as a function of drain voltage (V_{DS}) for several different gate voltages (V_{GS}). Here, the drain current conduction is studied with increasing drain voltage biases while the gate tunes the carrier density in the channel. In our FETs this measurement is primarily used to assess the contact quality, and the ohmic nature of the device. In addition, it can be used to extract parameters related to channel and contact resistances. The second current – voltage measurement involves measuring the drain current as a function of gate voltage (I_{DS} – V_{gs}) at constant drain voltage bias, shown in **Figure *2.19(b, c)***. The drain current is measured as the drain voltage drives carriers across the channel, while the gate voltage tunes the carrier density in the channel. Initially, the channel material is in the off-state. As the carrier density is tuned capacitively by the gate, the device transitions to the on-state. From this measurement device parameters, such as the field-effect mobility, subthreshold swing, and current on-off ratio can be determined.

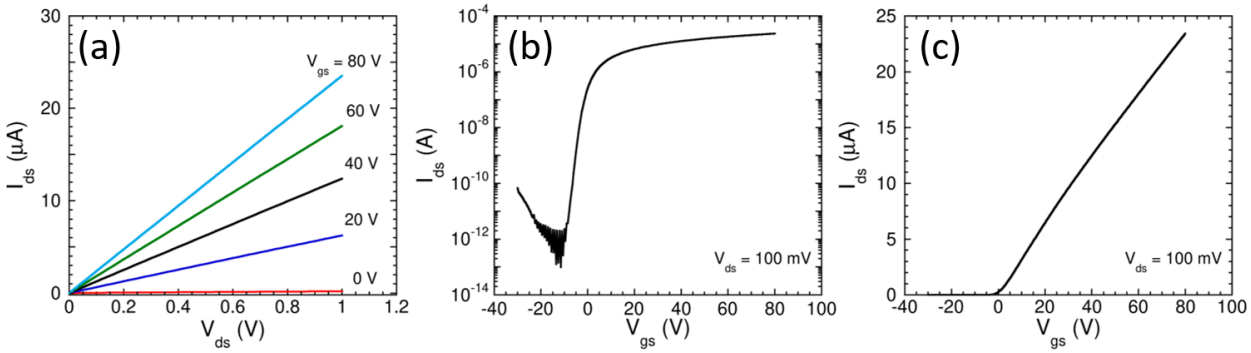

Figure 2.19 Example FET measurements. **(a)** Output curve produced by sweeping the drain bias (V_{ds}) and stepping the gate voltage bias (V_{gs}). **(b)** Semi-log and **(c)** linear transfer characteristics made by sweeping V_{gs} for a constant V_{ds}.

2.8 Nano-Squeegee

Despite attempts to minimize the amount of air traps between transferred samples at their respective interfaces, bubble formation is inevitable. These can be detrimental to device performance and thus intimate contact between successive layers of 2D materials is preferred. The annealing process described above can aid in the removal of bubbles that have formed during the fabrication process, but it is not effective enough. Recently, a new method for the removal of bubbles known as “nano-squeegeeing” has been shown to effectively create smooth, ultraclean atomic interfaces for 2D materials.[78] Nano-squeegeeing makes use of an AFM. Aside from the uses described in the previous section, an AFM can be used to apply a force to the sample surface. **Figure *2.20*** shows an illustration of the mechanism used in nano-squeegeeing, where the AFM tip is used to force bubbles trapped at the interface surface, pushing them toward the interface edge.

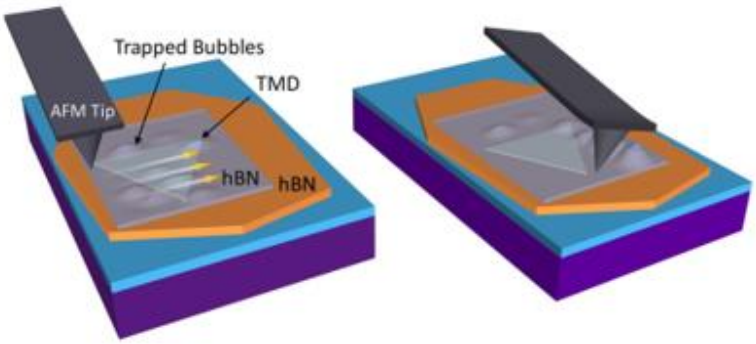

Figure 2.20 Cartoon illustration of how an AFM tip is used as a nano-squeegee to flatten TMD surfaces. Originally appeared in *Rosenberger et al., ACS Applied Materials and Interfaces,* (2018).[78]

Figure *2.21* shows an example of nano-squeegeeing a stack of 2D materials. In **Figure *2.21(a.1, 2)*** an initial scan is performed with a small amount of force (100 nN) to investigate the interface quality and identify areas with large amounts of bubble. Next, the force applied is increased (1000 nN) and applied over the surface. **Figure *2.21(b.1, 2)*** shows the result of the increased force. The bubbles have coalesced into some small clusters and some have also been pushed away from the critical interfaces. Clearly, the surface has been flattened. Further increasing the force, has an even greater effect as shown in **Figure *2.21(c.1,2 and d.1, 2)***. Eventually, the resulting interface surface is atomically smooth with no bubbles trapped between the materials leading to a superior interface quality as compared to the initial scan.

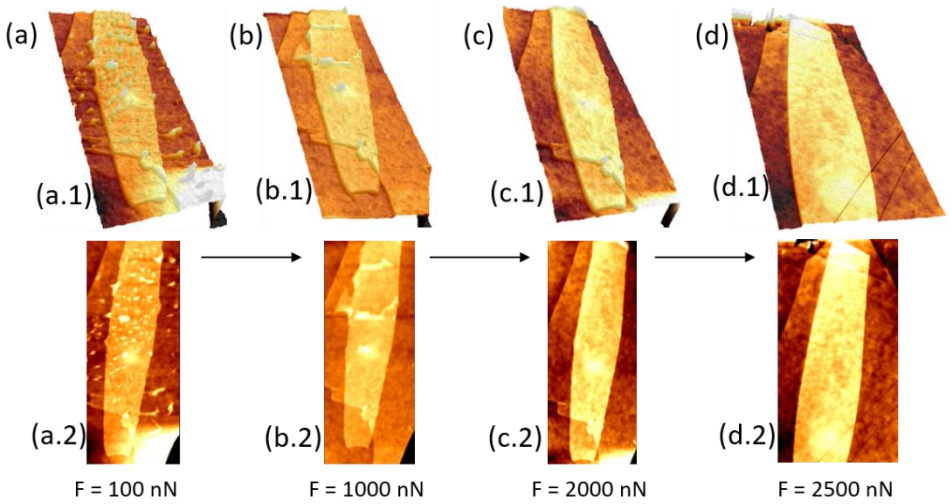

Figure 2.21 Example of nano-squeegee flattening on a stack of TMD flakes. **(a.1, 2)** An initial scan with low applied force is used to image the sample area. The force is then increased from 100 nN to **(b.1, 2)** 1000 nN, **(c.1, 2)** 2000 nN, and **(d.1, 2)** 2500 nN. With each progressive increase in the force, the air traps between the TMD layers are pushed toward the edges and eventually removed.

Chapter 3 CONTACT PROPERTIES OF 2D INTERLAYER FETs

3.1 Introduction

Layered 2D materials and TMDs have emerged in the post-graphene era of next-generation electronic materials as a promising candidate for use in low-power digital devices. They have many attractive properties, such as atomically smooth layers which reduce charge interface and roughness scattering, reasonable carrier mobility, and most importantly, a suitable bandgap. In addition, as a channel material in FETs TMDs offer the ability for ultra-short channel devices while mitigating SCEs required for the future growth of electronics.[32] Of the layered TMDs, the most studied are group VI TMDs. Group VI TMDs, such as MoS_2, WSe_2, and $MoSe_2$ are chemically and thermally stable which makes them realtively easy to fabricate in a typical research environment and ideal candidates for later integration into exisiting CMOS methods.[79, 80] Their bandgaps range from 1-2 eV, with a transition from indirect to direct with decreasing thickness. Despite the sizeable amount of research on these materials, a major impediment in understanding the intrinsic properties of them, and work toward the eventual commericial device applications with them is their tendency to form a substantial barrier with most commonly used metal for making electrical contacts.

The problem of barrier formation is further compounded by the phenomenom of FLP which reduces the effectiveness of choosing a metal with a favorable workfunction. In traditional FETs (e.g. Si, Ge, GaAs) the issue of contact barrier formation is dealt with by simply heavily doping the drain/source regions. In this way, the barrier depletion width is sufficiently thinned so that carriers can easily tunnel through it. Additionally, this method of heavily doping the drain/source regions, known as ion implantation, also deals with the

FLP effect in nearly all traditional semiconductors. However, while this method work extremely well for traditional semiconductor materials, it does not work well for 2D and TMD FETs. The reduced atomic thickness of 2D materials does not allow for an adequate doping profile. To combat this, the energy with which the doping process is performed can be increased, but this leads to sample damage.

To date, there have been many novel methods proposed and implemented to improves contacts to 2D FETs. Since the carrier injection into the FET channel is primarily dependent on the width and height of the Schottky barrier (SB) that forms at the contact interface, many of the contact strategies seek to reduce this barrier. The simplest approach would seem to be to choose a contact metal whose work function is similar to the electron affinity of the channel material, according to the Schottky-Mott model. Yet, the FLP mechanism prevents this from having much effect. Therefore, more novel approaches to reducing the SB height (SBH) and thus achieving ohmic contacts are needed. For example, phase-engineering works to transform the semiconducting layer at the contact interface of a device into metallic form while preserving the semiconducting nature of the channel material, or chemical doping methods work to achieve a heaving doping profile in the contacts to thin the SB.[56, 57, 59, 60, 62, 81] While these methods work relatively well to reduce the contact resistance by altering the SBH, they have issues which make them impractical for long-term applications or integration into larger-scale production. For example, they are are not thermally and chemically stable, are difficult to reliably control, or are not compatible with existing CMOS processing methods.

Recently, metal-oxides (e.g. TiO_2, Ta_2O_5, etc…) have been used as an interlayer material inserted between the semiconducting channel and the contact metal.[64-66] TiO_2

and Ta_2O_5 are particularly favorable as interlayer materials for MoS_2 FETs as they have similar electron affinities to MoS_2. The small difference in their electron affinities relative to that of MoS_2 is important for minimizing the tunneling barrier height and thus the tunneling resistance at the contacts. For example, the insertion of Ta_2O_5 between the contact metal and the MoS_2 channel can reduce the SBH to ~ 30 meV, which in turn results in a contact resistivity of $\sim 1 \times 10^5\ \Omega\,\mathrm{cm}^2$.[64] However the deposition of ultrathin, uniform metal-oxide materials on 2D materials is challenging due to their layered nature. To circumvent this challenge, 2D materials would be better candidates for interlayer materials as they can be assembled via vdW bonding without the need, for lattice matching, surface functionalization, or seeding layers.[82, 83] Ultrathin hBN has been demonstrated as an interlayer material for MoS_2 FETs, which resulted in a SBH of ~ 30 meV with a contact resistance of $\sim 1.8\ \mathrm{k}\Omega\,\mu\mathrm{m}$.[71] Although using hBN as an interlayer to MoS_2 FETs presents an approach that results in uniformity and removes the deposition challenges, hBN has a relatively large band offset with MoS_2 which means that there is a significant tunneling barrier acting in series with the SB. The addition of the large tunneling barrier severely hampers device performance despite the relatively small SBH and contact resistance. To achieve suitable device performance, removing the tunneling barrier is essential.

Thus far, the strengths and weakness of various insulating materials and a 2D interlayer, hBN has been examined, but it is worth exploring what makes a good candidate for use as an interlayer material. Material processing challenges aside, the most important parameter in determining a material's suitability as an interlayer is it relative band offset to the channel material, in this case MoS_2. Specifically, the difference between the

electron affinities (the difference between the conduction band edge and the vacuum energy) of the interlayer and the MoS_2 should be small to minimize the series tunneling resistance. Of course, this is a simplified picture, but it helps demonstrate why, for example Ta_2O_5 is well-suited as an interlayer while hBN is not. **Figure *3.1*** shows the band positions of several metal-oxides and some 2D materials including most of the group VI TMDs. It is evident now why a hBN interlayer introduces a large tunneling barrier due to the large offset between it and MoS_2. Conversely, the small difference shown between MoS_2 and TiO_2/Ta_2O_5 shows why the tunneling barrier is small in these cases. Interestingly, the group VI TMDs (e.g. WSe_2, $MoSe_2$) also have a relatively small band offset with MoS_2. This is important because unlike some of the metal-oxides, whose band alignment is favorable, group VI TMDs do not suffer from the processing issues that make it difficult to deposit them on MoS_2 as they can be assembled via vdW bonding similar to hBN. In this sense, the use of 2D semiconducting interlayers (e.g. group VI TMDs) combines the strengths of the favorable band alignments offered by metal-oxides to minimize the series tunneling resistance and the ease of fabrication and atomically smooth interface offered by hBN. Additionally, the prospect of a 2D semiconducting interlayer as a contact material to MoS_2 is particularly promising for scaling-up as this contact strategy can be utilized with current chemical vapor deposition (CVD) methods to achieve a large number of devices combined with existing CMOS fabrication techniques.

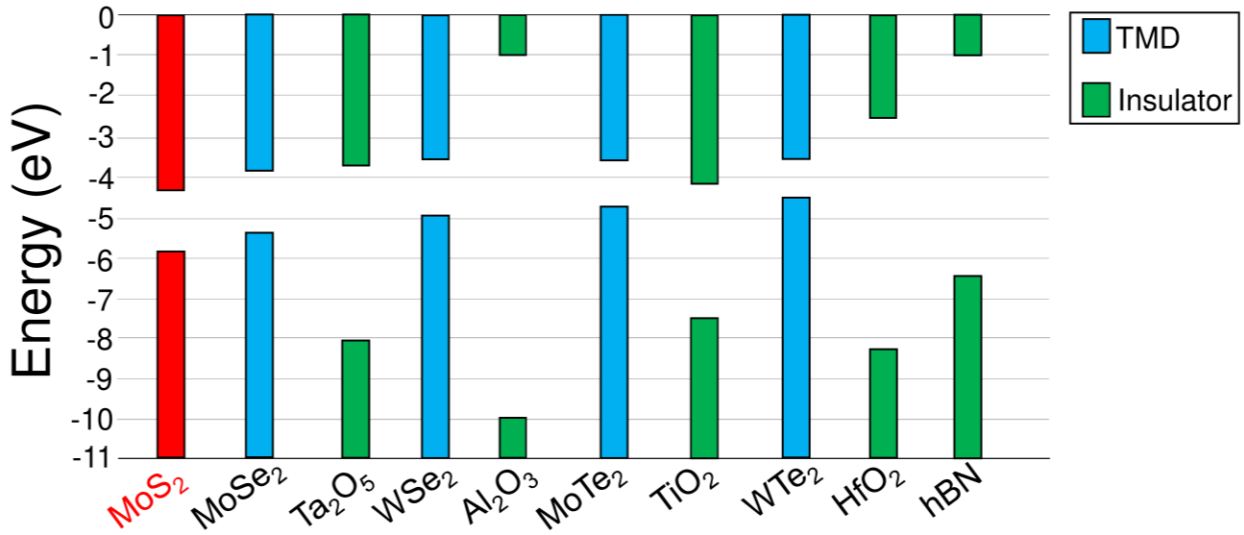

Figure 3.1 Band positions of various potential interlayer materials relative to MoS_2.

3.2 Semiconductor Interlayer Contacts Device Fabrication

Figure 3.2(a) presents an optical micrograph ***(panel i)*** and schematic ***(panel iii)*** of two MoS_2 FET devices fabricated on the same piece of few-layer MoS_2 channel material with and without a $MoSe_2$ interlayer at the contacts, respectively. ***Panel (ii)*** shows an AFM cross-sectional analysis of the 2.7 nm thick $MoSe_2$ interlayer in ***panel (i)***. To fabricate the FET devices, 10 – 30 nm thick hBN flakes exfoliated on degenerately doped Si with 280 nm of thermal oxide were used as ultra-flat and ultra-smooth substrate with minimum dangling bonds and charge traps. Next, mechanically exfoliated few-layer MoS_2 channel materials were placed on the hBN substrates by a dry transfer method. Subsequently, ultrathin $MoSe_2$ flakes were stacked on top of the MoS_2 channel also by the dry transfer method, serving as the interlayer at the drain/source contacts. Here two $MoSe_2$ flakes of identical thickness (2.7 nm) were exclusively placed in the drain/source regions (while leaving the channel region uncovered) to exclude the possibility of the $MoSe_2$ interlayer influencing the channel properties. Finally, metal electrodes, consisting

of 10 nm Ti and 40 nm Au, were fabricated on top of the drain/source regions of the MoS_2 channel with and without $MoSe_2$ interlayer by electron beam lithography and electron beam assisted metal deposition.

3.3 Transfer Characteristics of MoS_2 Devices with Interlayers

To measure the electrical properties of the MoS_2 FET devices, back-gate biases were applied through the SiO_2/hBN dielectric stack to tune the carrier density in MoS_2. ***Figure 3.2(b)*** shows the room-temperature transfer characteristics of the two MoS_2 FETs with and without a $MoSe_2$ interlayer beneath the Ti electrodes with drain/source voltage V_{ds} = 1 V. To account for the differences in the channel length (L) and width (W) between the two devices, width and length normalized current $I_{ds} \times L / W$ was plotted to quantitatively compare their transfer characteristics. While both devices display *n*-type behavior, the transfer curve of the device with direct Ti contacts plotted on linear scale is shifted by ~ 25 V to the right. This threshold voltage shift cannot be simply explained by sample-to-sample variations (e.g. doping and thickness differences) because both devices were fabricated from the same MoS_2 flake with uniform thickness and on the same hBN substrate. The only difference between them is that two ~2.7 nm thick $MoSe_2$ flakes were inserted at the drain and source contacts as interlayers in one of the devices, suggesting that the current in the MoS_2 with direct Ti contacts in the low gate voltage region (-10 < V_{gs} < 15V) is strongly suppressed by a substantial contact barrier and that the insertion of a $MoSe_2$ interlayer at the Ti contacts significantly reduces this barrier. The semi-log plot of the transfer curve for the MoS_2 device with direct Ti contacts exhibits an intermediate gate-voltage region between the thermionic emission limited subthreshold region and the on-state region, which can be attributed to thermally assisted tunneling

through a SB.[84] This thermally assisted tunneling region overlaps with the region of suppressed drain current on the linear plot, confirming the presence of a significant SB at the direct Ti/MoS_2 contacts. As the SBH decreases, higher thermionic current can be reached before the thermally assisted tunneling current becomes dominant. The near absence of such a thermally assisted tunneling region in the MoS_2 device with Ti/$MoSe_2$ contacts strongly suggests a significantly reduced SBH. ***Figure 3.2(c, d)*** shows the output characteristics of the two devices normalized by the device length and width. Although both devices exhibit linear *I-V* characteristics at high gate voltages, the *I-V* curves of the MoS_2 device with direct Ti contacts is significantly more non-linear and asymmetric than the device with Ti/$MoSe_2$ contacts (see the ***inset of Figure 3.2 c, d***) at low gate voltages, further indicating a more significant SB in the former than in the latter. In addition, the overall normalized output current is a factor of two larger in the device with Ti/$MoSe_2$ contacts, which is consistent with the SBH reduction.

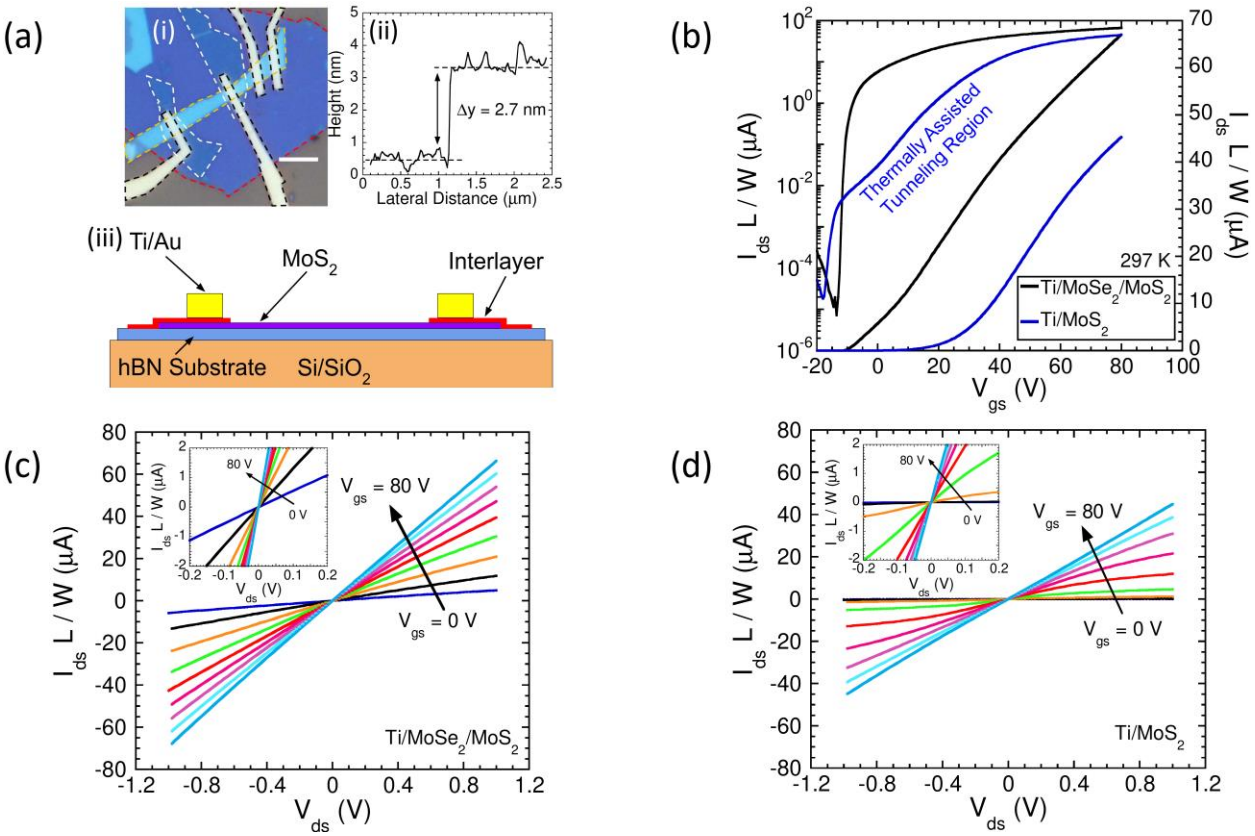

Figure 3.2 Device structure and characteristic of MoS_2 FETs with direct Ti and Ti/$MoSe_2$ interlayer contacts. **(a)** (i) Optical micrograph of a FET with a 7.7 nm MoS_2 (orange dashed lines) channel fabricated on a 18 nm hBN substrate (red dashed lines) and 280 nm SiO_2 substrate with 2.7 nm $MoSe_2$ interlayers (white dashed lines) as drain/source electrodes and 10/40 nm Ti/Au metal electrodes (black dashed lines) deposited for comparison of direct Ti and Ti/$MoSe_2$ contacts, (ii) AFM cross-sectional analysis of the $MoSe_2$ interlayer in panel (i), (iii) Shows a side-view schematic of a MoS_2 FET with interlayer contacts. **(b)** Measured room temperature transfer curves comparing FETs with direct Ti and Ti/$MoSe_2$ contacts. The semi-log drain/source current is normalized by device length (L) and width (W) to compare different device geometries. The MoS_2 FET with direct Ti contacts displays a large thermally assisted tunneling region, consistent SB limited contacts. **(c, d)** Room-temperature normalized output characteristic for **(c)** Ti/$MoSe_2$ and **(d)** direct contacts on MoS_2. The low drain bias regions are shown in the insets of **(c)** and **(d)**.

Figure *3.3(a)* shows transfer characteristics of a MoS_2 FET with asymmetric contacts: direct Ti contact on one end of the channel and Ti/$MoSe_2$ contact on the other end. Two prominent features can be observed in the transfer characteristics of this MoS_2 device: (1) the current is substantially reduced when the direct Ti contact is biased as the source; and (2) the threshold voltage is shifted to the right in this bias configuration. Here

the MoS_2 device can be modeled as two back-to-back Schottky diodes connected by a MoS_2 channel, where the source contact is reverse biased while the drain contact is forward biased. At sufficiently large drain-bias of V_{ds} = 1 V, the reverse biased Schottky contact is much more resistive than the forward biased Schottky contact. Because the transfer characteristics in **Figure *3.3(a)*** were measured on the same device, the discrepancies in current and threshold voltage can be unequivocally attributed to the larger SBH at the direct Ti contact. The difference in SBH between the Ti/$MoSe_2$ and direct Ti contacts also leads to rectifying *I-V* output characteristics as shown in **Figure *3.3(b)***. These results provide further support to the conclusions drawn from **Figure *3.2***.

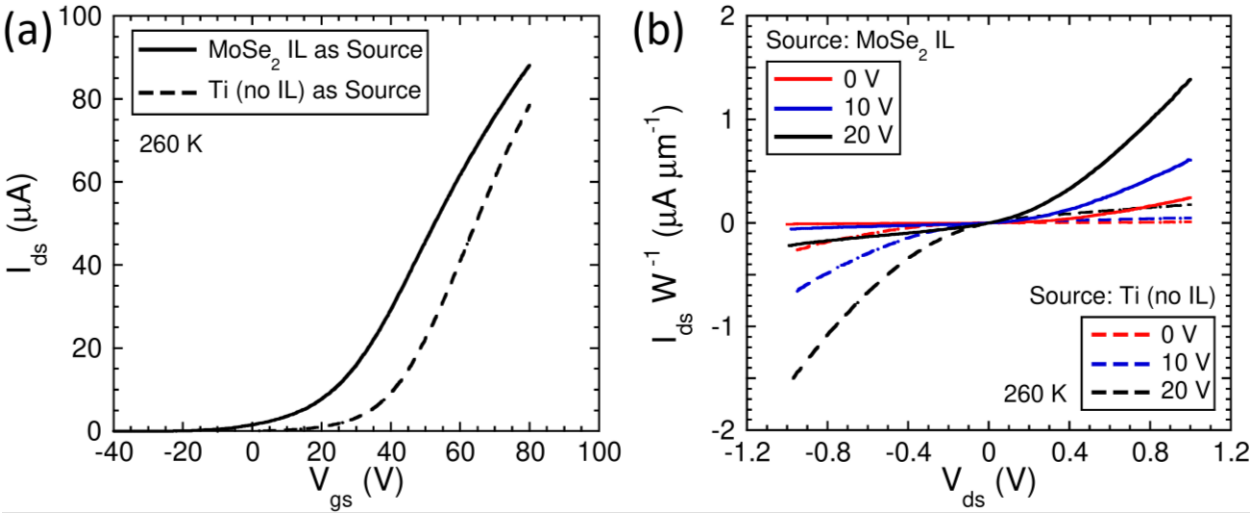

Figure 3.3 (a) Transfer and **(b)** output curves comparing Ti/$MoSe_2$ (solid curve) and direct Ti (dashed curve) contacts as the source electrode to a MoS_2 channel.

Based on **Figure *3.1*** $MoSe_2$ offers a favorable band offset with MoS_2, but there are also other group VI TMDs whose band offset is also favorable, such as WSe_2. ***Figure 3.4(a)*** shows the transfer characteristics of two MoS_2 FETs fabricated on the same uniform channel but with different contacts: direct Ti contacts on one device and Ti/WSe_2 contacts on the other. Similar to MoS_2 FETs with Ti/$MoSe_2$ contacts, the device with Ti/WSe_2 contacts also shows improved normalized current (normalized to *L/W*) and more

negative threshold voltage in comparison with the device with direct Ti contacts, which is consistent with a lower SBH. In addition, the device with Ti/WSe_2 contacts also exhibits higher and more linear output currents as shown in ***Figure 3.4(c)*** compared to that with direct Ti contacts (shown in ***Figure 3.4 b***).

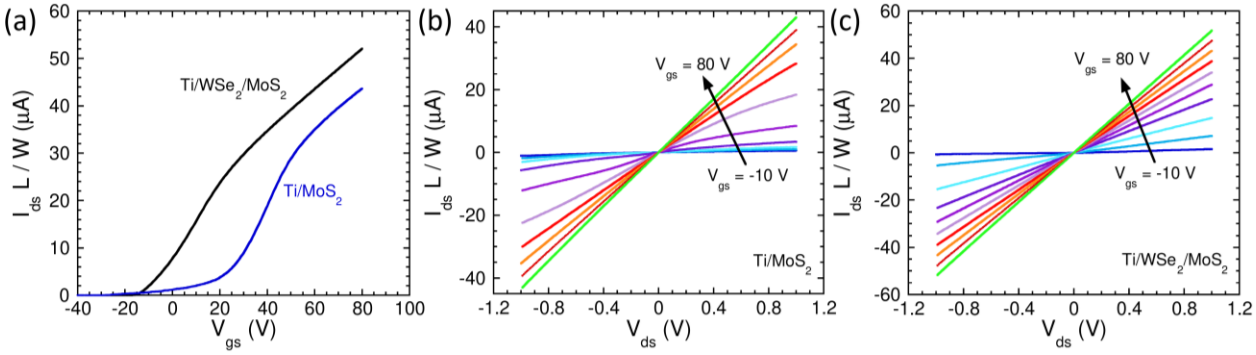

Figure 3.4 (a) Transfer curve comparing Ti/WSe_2 (black curve) and direct Ti (blue curve) contacts to a MoS_2 FET on a hBN/SiO_2 back-gated substrate. Normalized output characteristics for **(b)** direct Ti and **(c)** Ti/WSe_2 contacts.

3.4 Schottky Barrier Height Extraction

To quantitatively assess the impact of 2D semiconductor interlayers on the SBH, we have extracted the activation energy from the slope of an Arrhenius plot of $\ln(I_{ds}/T^{3/2})$ versus 1000/T for MoS_2 FETs.[71, 85] MoS_2 FETs are modeled as two back-to-back Schottky diodes connected by a MoS_2 channel; and our SBH extraction method is based on the thermionic emission current through a reverse-bias Schottky diode at the flat-band voltage.[86] The thermionic emission current density is given by[20]

$$I_{DS} = A_{2D}^{*} T^{3/2} e^{\left(-\frac{q\Phi_B}{k_B T}\right)} \left[1 - e^{\left(-\frac{qV}{k_B T}\right)}\right], \qquad (\mathbf{3.1})$$

where A_{2D}^{*} is the 2D Richardson's contacts ($= 4\pi q k_B^2 m^*/h^3$), T is the temperature, q is the electron charge, V is the applied voltage at the junction, and Φ_B is the barrier height

defined as the energy difference from Fermi level of the contact metal to the conduction band of the semiconductor (for *n*-type semiconductors).

To extract the Schottky barrier height (SBH), the drain voltage is biased such that $|qV| \gg k_B T$, which makes the term in brackets in ***equation 3.1*** ≈ 1 for the reverse-bias Schottky contact. Rearranging ***equation 3.1*** and taking the natural log of $I_{ds}/T^{3/2}$ yields:

$$ln\left(\frac{I_{DS}}{T^{3/2}}\right) = ln(A_{2D}^{*}) - \Phi_B\left(\frac{q}{k_B T}\right). \qquad (\mathbf{3.2})$$

From ***equation 3.2***, the slope of $\ln\left(\frac{I_{ds}}{T^{3/2}}\right)$ is proportional to the extracted Φ_B for a given gate voltage. Since the gate voltage is effectively tuning the charge doping in the junction, thermally assisted tunneling and tunneling current through the SB may become significant at high positive gate voltages (carrier densities) for an electron SB. In this case, the extracted $\Phi_B$based on the themionic emission model is expected to be smaller than the actural SBH. On the other hand, an increasingly negative gate voltage increases the channel barrier height, which consequently leads to a higher extracted Φ_B. The extracted Φ_B becomes the true SBH at the flat-band voltage, above which the extracted Φ_B as a function of gate voltage deviates from its linearity (at lower gate voltage).

3.4.1 Schottky Barrier Height with Interlayer Contacts to MoS_2

Figure *3.5(a, b)* shows the Arrhenius plots of two presentative MoS_2 FETs with and without interlayers inserted at the metal contacts, respectively. The extracted activation energy is plotted as a function of gate voltage for the devices with (**Figure *3.5 c***) and without a $MoSe_2$ interlayer (**Figure *3.5 d***). The SBH is determined as the activation energy at the flat band voltage, the point above which the activation energy starts to

deviate from the linear dependence of the gate voltage. Above (more positive than) the flat band voltage, thermally assisted tunneling current across the SB can no long be ignored, leading to a weaker dependence of the extracted activation energy on the gate voltage. Using this technique, SBHs of 95 meV and 26 meV are determined for the direct Ti/MoS_2 and Ti/$MoSe_2$/MoS_2 contacts, respectively. We have measured the SBH of multiple MoS_2 devices with and without $MoSe_2$ interlayers at the contacts. While the SBH of direct Ti/MoS_2 contacts varies from 95 to 117 meV, the SBH of Ti/$MoSe_2$/MoS_2 falls into a narrow range of 25 – 30 meV.

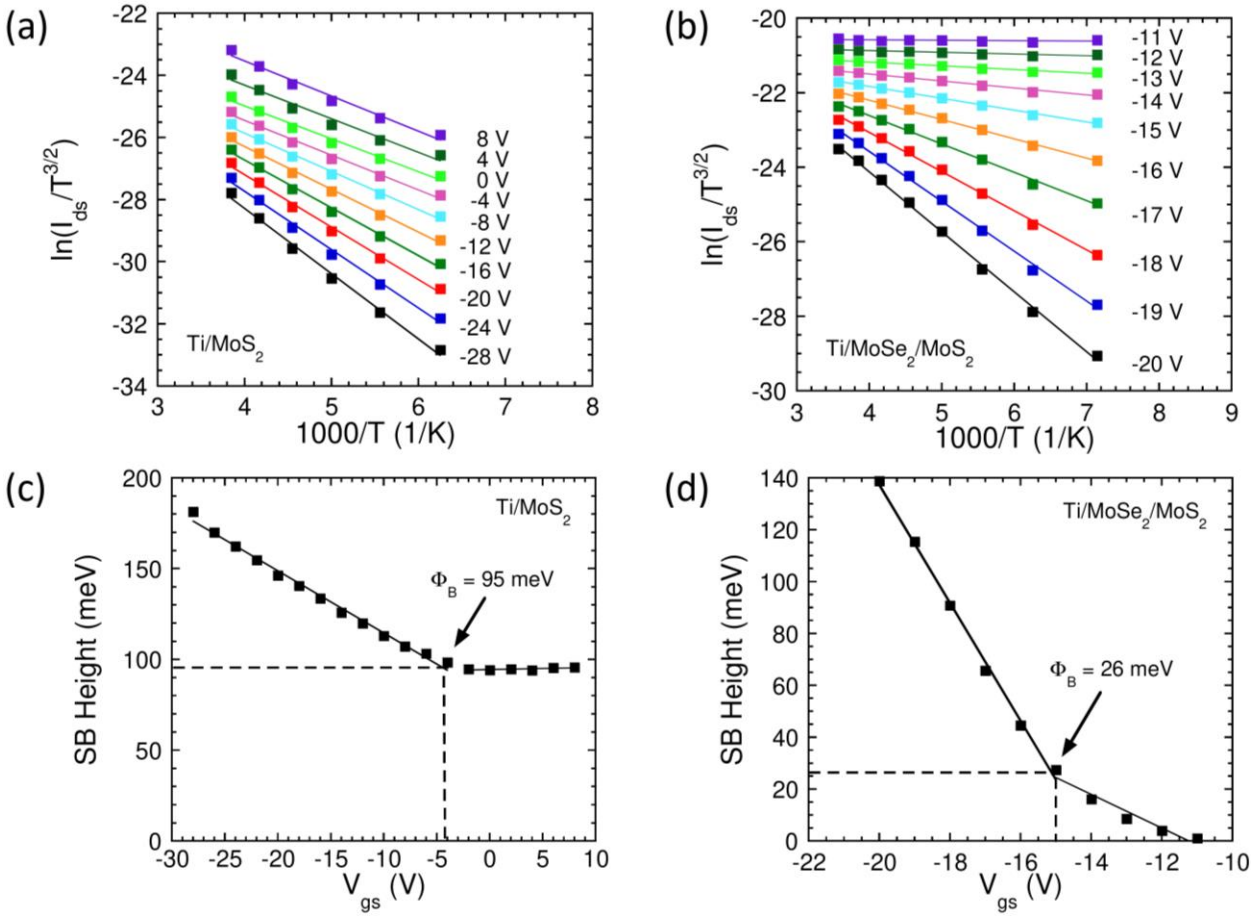

Figure 3.5 Flat-band Schottky barrier height extraction. **(a, b)** Arrhenius plots of **(a)** direct Ti and **(b)** Ti/$MoSe_2$ contact to MoS_2 for various gate voltages. **(c, d)** The extracted n-type SBH at various gate voltage, where the flat-band SB is measured to be **(c)** 95 meV and **(d)** 26 meV in direct Ti and Ti/$MoSe_2$ contacts, respectively.

In addition to Ti/$MoSe_2$ contacted MoS_2 FETs, other 2D materials such as WSe_2, Re-doped WSe_2, and hBN are also used as interlayer materials to make Ti/WSe_2, Ti/$ReWSe_2$, and Ti/hBN contacts to MoS_2 FETs. As shown in ***Figure 3.6*** all these interlayer materials reduce the SBH to ~ 50 meV or slightly less in MoS_2 devices. However, the SBHs using Ti/WSe_2, Ti/$ReWSe_2$, and Ti/hBN contacts are still much higher than the SBHs in Ti/$MoSe_2$ contacted MoS_2 devices.

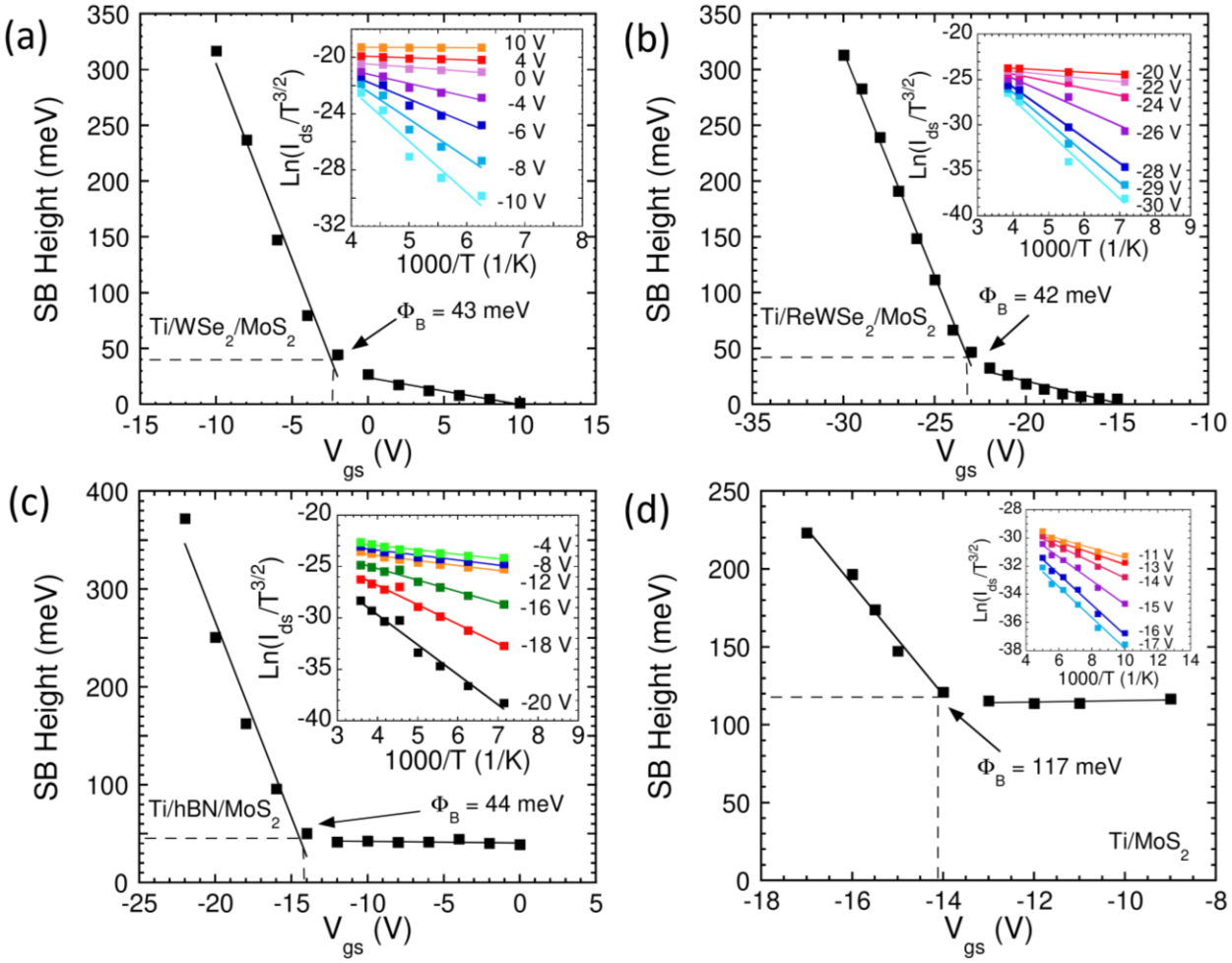

Figure 3.6 The extracted SBH at various gate voltages and Arrhenius curves **(insets)**, where the flat-band electron SBH is shown for **(a)** Ti/WSe_2, **(b)** Ti/$ReWSe_2$, **(c)** Ti/hBN, and **(d)** direct Ti contacts to MoS_2 FETs.

In addition to Ti, we also directly deposited Au (without Ti adhesion layer) as the contact metal to further elucidate the underlying mechanism of SBH reduction. In spite of

the much larger work function of Au (~ 5.1 eV) than Ti (~ 4.3 eV), the addition of an $MoSe_2$ interlayer at the contacts lowers the SBH as shown in **Figure *3.7***, effectively ruling out Fermi-level depinning as dominant mechanism of SBH reduction.

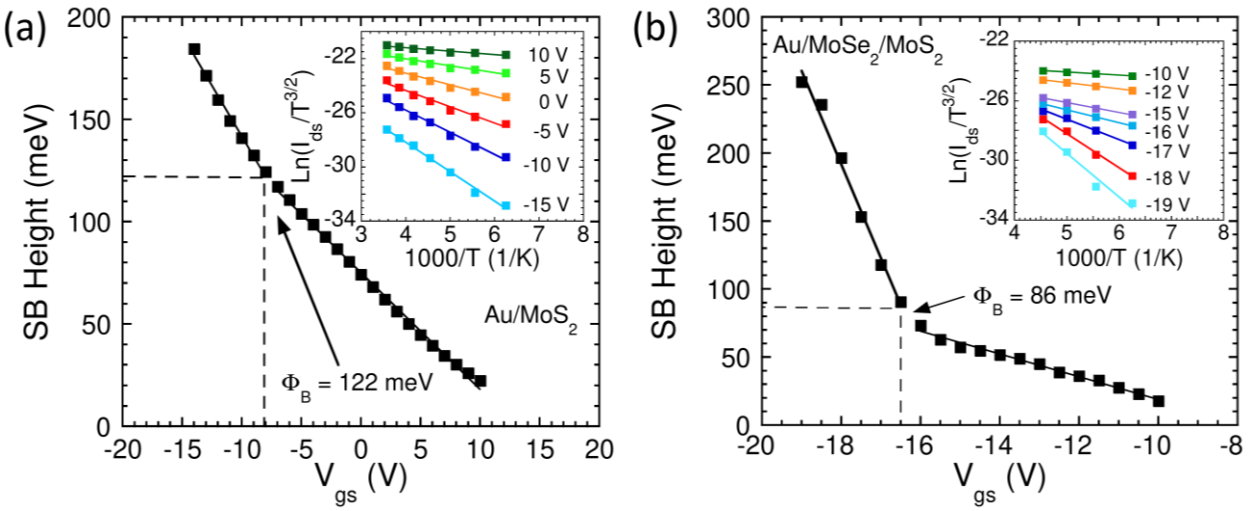

Figure 3.7 The extracted SBH at various gate voltages and Arrhenius curves **(insets)**, where the flat-band electron SBH is shown for **(a)** direct Au and **(b)** Au/$MoSe_2$ contacts to MoS_2 FETs.

To shed light on the SBH lowering mechanism in our MoS_2 devices with metal-semiconductor-semiconductor (MSS) contacts, we have systematically measured the SBH of multiple devices with different interlayer materials, varying interlayer thicknesses and doping concentrations, and different contact metal work functions as summarized in **Figure *3.8(a)***. Several different mechanisms have been proposed to explain the reduction of SBH in metal-insulator-semiconductor (MIS) contacts including attenuation of metal induced gap states (MIGS), formation of electronic dipole at the insulator-semiconductor interface, passivation of interfacial defects, and interfacial doping. [64, 71, 87, 88] For both Ti/$MoSe_2$ and Ti/WSe_2 contacts, the SBH is nearly independent of the interlayer thickness in the range of 1.3 - 6 nm, which is contrary to the MIGS attenuation mechanism because MIGS are expected to decay with increasing interlayer thickness.[89]

The nearly factor of two difference in the SBH between Ti/$MoSe_2$/MoS_2 and Ti/WSe_2/MoS_2 contacts cannot be explained by the passivation of interfacial defects either.

To investigate the effects of interfacial dipole on the SBH reduction, we compared the SBH of MoS_2 devices using undoped WSe_2 and *n*-doped $Re_{0.005}W_{0.995}Se_2$ (with an electron centration of ~ 6×10^{17} cm^{-3}) as interlayers, respectively.[90] Variations of the carrier concentration shift the Fermi level of the interlayer materials, which is expected to modify the interfacial dipole between the interlayer and the channel due to charge transfer between them. However, MoS_2 devices with undoped WSe_2 and *n*-doped $Re_{0.005}W_{0.995}Se_2$ show comparable SBH, indicating that the interfacial dipole is unlikely a dominant contributor to the SBH reduction. The lack of interlayer doping dependence in the SBH can be attributed to the pinning of metal Fermi-level to the CNL of the interface gap states in the interlayer. The Fermi level of an ultrathin 2D semiconductor interlayer is also expected to be equivalent to its CNL, which is primarily determined by MIGS and defects induced during the metal deposition rather than by the bulk doping concentration.[87]

After ruling out Fermi-level depinning and/or interfacial dipole as dominant SBH lowering mechanisms in our MoS_2 devices with 2D semiconductor interlayers, we propose a new SBH lowering mechanism unique to metal/2D-semiconductor/2D-semiconductor contacts. **Figure *3.8(b, c)*** shows band diagrams of Ti/$MoSe_2$/MoS_2 and Ti/MoS_2 contacts. As schematically shown in **Figure *3.8(b)***, the Fermi level of Ti metal is pinned to the CNL of $MoSe_2$ interlayer relatively close to its conduction band edge; and the conduction band edge of $MoSe_2$ interlayer lies above that of MoS_2 channel because

the electron affinity of $MoSe_2$ is smaller than that of MoS_2.[91] In this way, the new SBH between the Ti metal and MoS_2 channel now follows:

$$\Phi_B = \Phi_{IL} - (\chi_{CH} - \chi_{IL}), \qquad (\mathbf{3.3})$$

where Φ_B is the SBH between metal and channel, Φ_{IL} the tunneling barrier height of the interlayer, χ_{CH} and χ_{IL} the electron affinity of the channel and interlayer materials, respectively. The Φ_{IL} for the $MoSe_2$ is expected to be similar to the SBH between Ti and $MoSe_2$ (which is comparable to the SBH between Ti and $MoSe_2$) because both of them are determined by the Fermi level pinning to the CNL of $MoSe_2$. Average SBH of Ti/$MoSe_2$ contacts is about 130 meV (see **Figure *3.9***), which is only ~ 30 meV higher than that of direct Ti/MoS_2 contacts. However, the electron affinity of $MoSe_2$ is on the order of 100 meV smaller than that of MoS_2, which is expected to lower the conduction band edge of the MoS_2 with respect to the Fermi level by a similar amount.[92] Consequently, a substantially lower SBH is achievable in Ti/$MoSe_2$/MoS_2 than in direct Ti/MoS_2 contacts (as shown in **Figure *3.8 c***). In the case of Ti/WSe_2/MoS_2 contacts, on the one hand, the CNL of WSe_2 lies further away from its conduction band edge and closer to the middle of the band gap.[93] On the other hand, the conduction band offset between WSe_2 and MoS_2 is larger than that between $MoSe_2$ and MoS_2.[94] These two competing factors combine to result in an overall reduction of the SBH after inserting the WSe_2 interlayer. It is worth noting that the SBH of Ti/$MoSe_2$/MoS_2 contacts is also substantially smaller than that of Ti/hBN/MoS_2 contacts (also see ***Figure 3.6 c***). Moreover, both the tunneling barrier height and the SBH are further reduced by the charge image lower effects, which are enhanced by the ultrathin interlayer. The relatively low tunneling barrier height of $MoSe_2$ interlayer is ideal for reducing the series tunneling resistance of the Ti/$MoSe_2$/MoS_2

contacts because the resistance of the tunneling barrier in the low-voltage bias (direct tunneling) region follows:

$$R_T \propto exp\left(-2\Delta s\sqrt{2m^*\Phi}/\hbar\right), \qquad (\mathbf{3.4})$$

where m^* is the electron effective mass, $\hbar$ is the reduced Planck constant, and Φ and Δs are the effective barrier height and width, respectively.

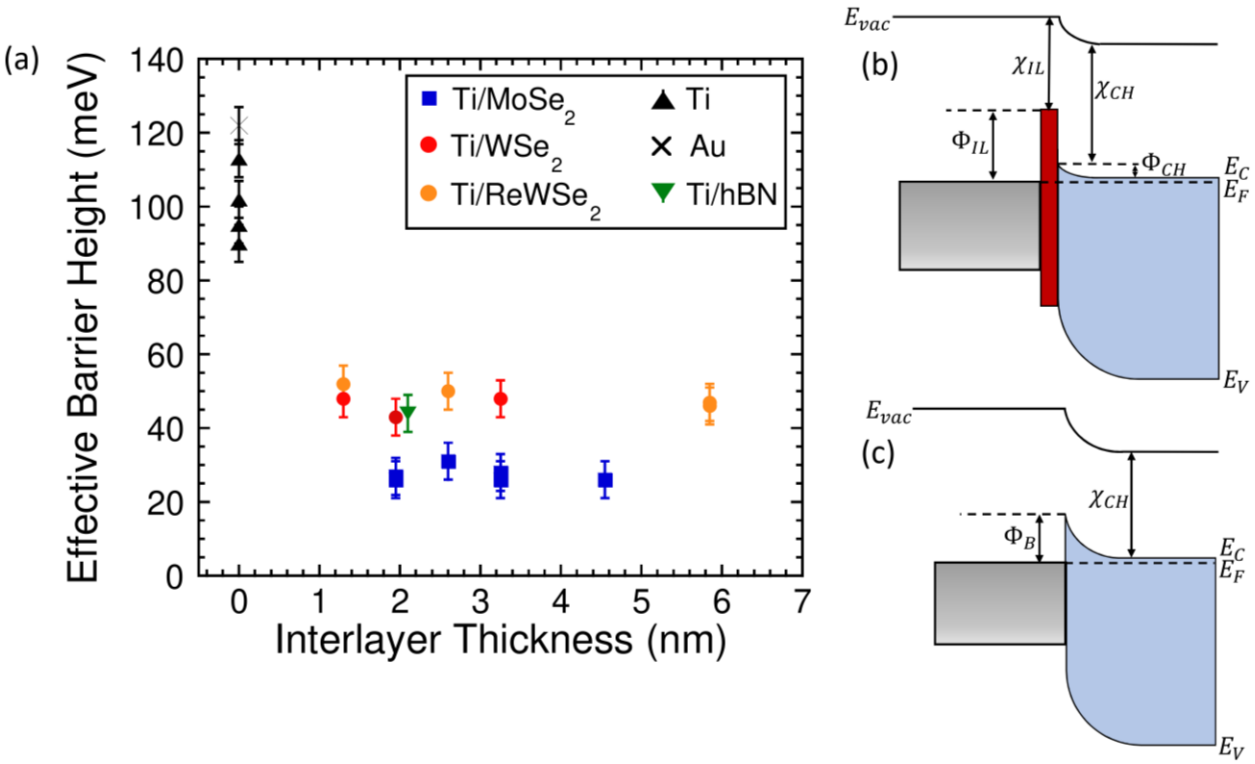

Figure 3.8 Extracted SBH and band alignments of interlayer devices. **(a)** The extracted barrier height from MoS_2 FETs using several contact metals and different interlayer materials. Barrier from direct metal contacts is nearly the same despite drastically different metal work functions ($\Phi_{Ti} = 4.3\ eV$ and $\Phi_{Au} = 5.1\ eV$) indicating a strong Fermi level pinning effect in direct contacts to MoS_2. By inserting a 2D interlayer with an advantageous band alignment the barrier height can reduced significantly in MoS_2 to ~ 50 meV (using WSe_2 and $ReWSe_2$ interlayers) and further to ~ 25 meV (using $MoSe_2$ interlayer) regardless of the interlayer thickness. **(b, c)** Illustrations of the band alignments in MoS_2 FETs with an **(b)** interlayer inserted between the contact metal and the MoS_2 channel and **(c)** direct metal contacts. With interlayer contacts the channel SBH (Φ_B) can estimated according to $\Phi_B = \Phi_{IL} - (\chi_{IL} - \chi_{CH})$, where Φ_{IL} is the tunneling barrier height of the interlayer, and χ_{IL} and χ_{CH} are the electron affinities of the interlayer material and channel, respectively.

Along with MoS_2 FETs, we have also fabricated FETs using $MoSe_2$ as the channel material. As shown in **Figure *3.9***, the insertion of a MoS_2 interlayer increases the electron SBH of Ti contacted $MoSe_2$ FETs, which is in sharp contrast to SBH reduction observed in Ti/$MoSe_2$ contacted MoS_2 devices. The SBH increase due to the MoS_2 interlayer can also be attributed to same mechanism that explains the SBH reduction in MoS_2 devices with Ti/$MoSe_2$ contacts. Because the electron affinity of MoS_2 is larger than that of $MoSe_2$, the combination of conduction band-offset and Fermi-level pinning to the MoS_2 interlayer increases the SBH.

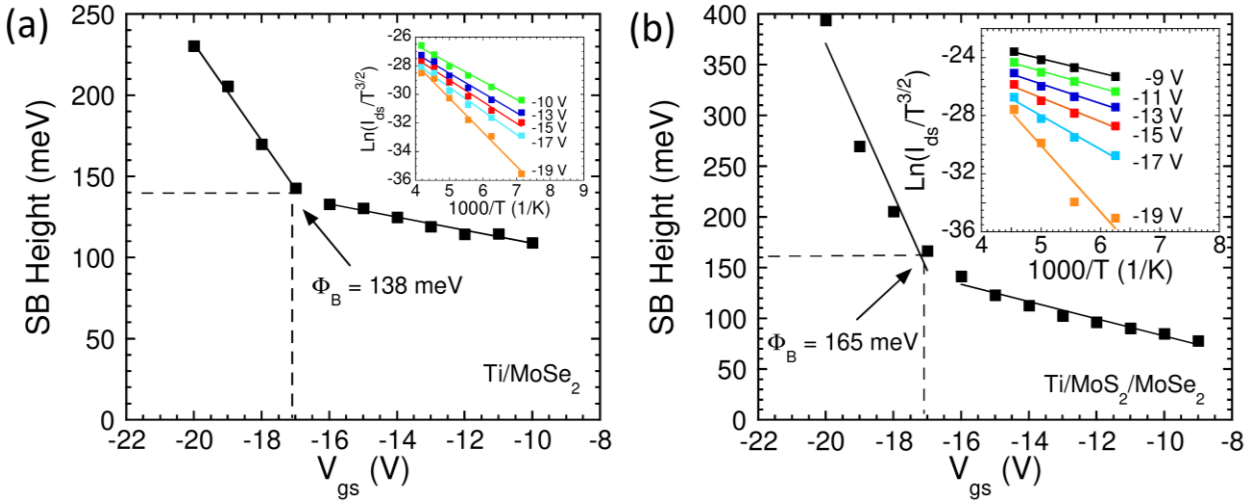

Figure 3.9 The extracted SBH at various gate voltages and Arrhenius curves **(insets)**, where the flat-band electron SBH is shown for **(a)** direct Ti and **(b)** Ti/MoS_2 contacts to $MoSe_2$ FETs.

3.5 Contact Resistance, Resistivity, and Transfer Length

3.5.1 Evaluation of Contact Resistance in MoS_2 Devices with Interlayers

To quantitatively understand the impact of reduced SBH on the contact resistance, transfer length method (TLM) was used to extract the contact resistance of MoS_2 FETs with and without contact interlayers. This is achieved by fabricating devices with multiple patterned channel lengths of increasing size. The total resistance (normalized by device width) in these devices can be modeled as a function of channel length

$$R_{Total} = L_{ch}R_{sh} + 2R_{\mathrm{C}}. \qquad (\mathbf{3.5})$$

Here, when plotting R_{Total} as a function of channel length, the slope of the linear fit yields the sheet resistance R_{sh} and the contact resistance can be extracted from half of the *y*-intercept (as shown in **Figure *3.10 d***). A diagram of the TLM device structure used to perform the measurement is shown in the ***inset of*** **Figure *3.10(d)***. **Figure *3.10(a)*** shows the output characteristics of MoS_2 devices with Ti/$MoSe_2$/MoS_2 contacts and different channel lengths at V_{gs} = 80 V. Similarly, the output characteristics of two other MoS_2 devices with Ti/WSe_2/MoS_2 and direct Ti/MoS_2 contacts, were shown in **Figure *3.10(b, c)***, respectively. The $MoSe_2$ and WSe_2 interlayers were both about 2nm thick. The total resistance normalized by width (R_{total}) was obtained from the slope of the *I-V* characteristics and plotted as a function of channel length in **Figure *3.10(d)***. The excellent linear fit to the data of all three devices indicates low variability among the contacts and channels for each device. The *y*-intercept of the linear fit yields the total contact resistance $2R_c$ and the slope gives the sheet resistance R_{sh} of the MoS_2 channel in each device. The TLM measurements at V_{gs} = 80 V yield a contact resistance of 1.9 kΩ μm for the Ti/$MoSe_2$/MoS_2, 6.5 kΩ μm for the Ti/WSe_2/Au and 14.5 kΩ μm for the Ti/MoS_2 contacts, which is qualitatively consistent with their respective SBH disparities. The order of magnitude difference in the contact resistance between Ti/$MoSe_2$/MoS_2 and Ti/MoS_2 contacts is maintained the carrier concentration (gate bias voltage) decreases as illustrated in **Figure *3.10(e)***. On the other hand, the sheet resistance exhibits much smaller variations among the three devices in spite of the large variations in the contact resistance (see **Figure *3.10 f***).

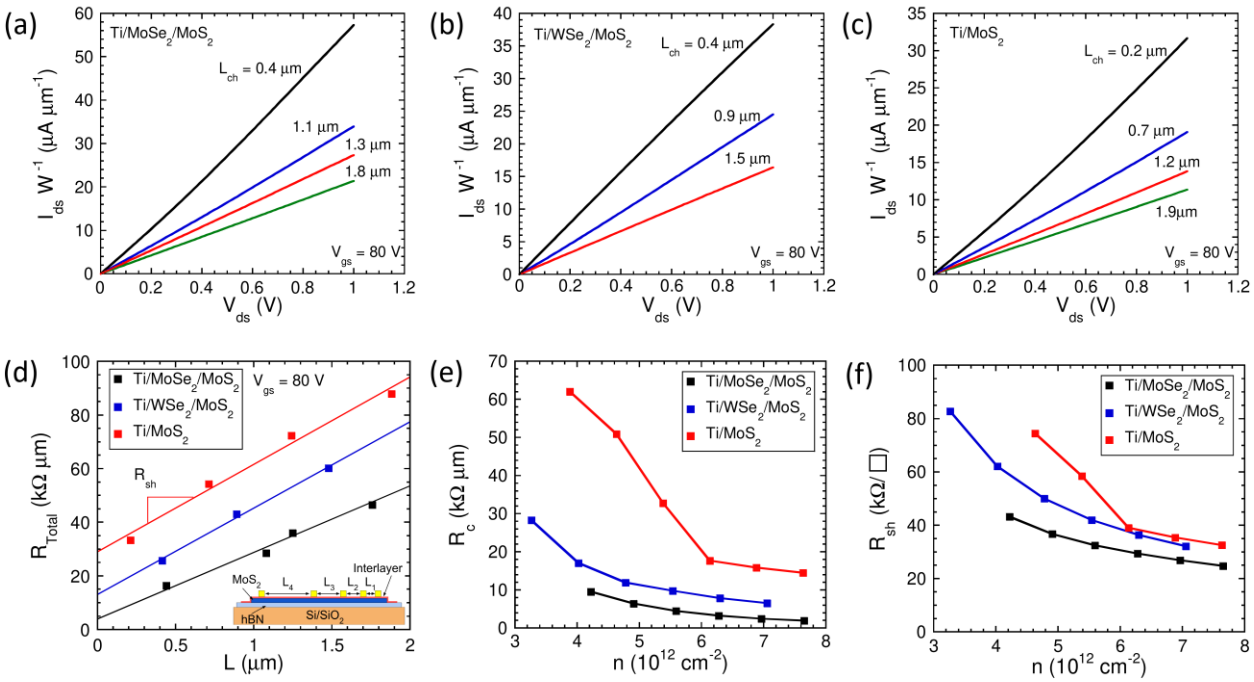

Figure 3.10 Contact properties of MoS_2 FETs with direct and interlayer contacts**. (a-c)** Room temperature normalized I_{ds}-V_{ds} output curves for different channel length at V_{gs} = -80V for **(a)** Ti/$MoSe_2$, **(b)** Ti/WSe_2, and **(c)** direct Ti contacts. **(d)** The total resistance normalized by width (R_{total}) as a function of channel length for each contact type determined by the slopes from **(a-c)** at V_{gs} = -80 V. The y-intercept yields twice the contact resistance ($2R_C$), and slope yields the total sheet resistance (R_{sh}). The **inset** of **(d)** shows a side-view schematic of the structure used in TLM measurements. **(e, f)** Comparison of **(e)** extracted contact resistance and **(f)** sheet resistance for each contact type as function of carrier density (gate voltage bias).

3.5.2 Extraction of Contact Resistivity and Transfer Length

The overall miniaturization of 2D semiconductor electronic devices requires not only reduced channel length but also shorter contact length (L_C) without increasing the contact resistance. In order to simultaneously accomplish these goals, it is important to concurrently achieve low contact resistivity and small current transfer length (L_T, the characteristic length over which the current is injected). ***Figure 3.11*** shows the carrier density dependent contact resistivity (***Figure 3.11 a***) and transfer length (***Figure 3.11 b***) extracted from R_C and R_{sh},

$$L_T = \sqrt{\frac{\rho_C}{R_{sh}}}, \qquad (\mathbf{3.6})$$

in conjunction with the transmission line model,[58]

$$R_C = \frac{\rho_C}{L_T} coth\left(\frac{L_C}{L_T}\right). \qquad (\mathbf{3.7})$$

The **inset of *Figure 3.11(b)*** schematically illustrates the decay of injected current over the transfer length. The Ti/$MoSe_2$/MoS_2 contacts exhibit the lowest contact resistivity of $\rho_C \approx 1.1 \times 10^{-6} \Omega\, cm^2$ at the highest carrier concentration, which is ~60 times lower than Ti/MoS_2 contacts and several times lower than Ti/WSe_2/MoS_2 contacts. The contact resistivity obtained in our Ti/$MoSe_2$/MoS_2 contacts is also 1-2 orders of magnitude lower than Ti/Ta_2O_5/MoS_2 with a 1.5 nm thick Ta_2O_5 interlayer and similar effective SBH, possibly due to a lower tunneling barrier of the $MoSe_2$ interlayer.[64] With a smaller contact resistivity, the current is preferably injected near the contact edge, leading to a smaller transfer length. The transfer length of our Ti/$MoSe_2$/MoS_2 is ~ 60 nm, which is more than 5 times smaller than that of Ti/MoS_2 contacts. As the carrier density decreases, the contact resistivity increases due to reduced field emission and/or thermal field emission current through the effective SB. Accordingly, the transfer length increases with decreasing carrier density responding to increasing contact resistivity and sheet resistance. It is worth noting that the average contact length is 1 μm in the Ti/$MoSe_2$/MoS_2 device which is over an order of magnitude larger than the current transfer length, indicating that current crowding is a negligible factor in electrical measurements even at low carrier densities.

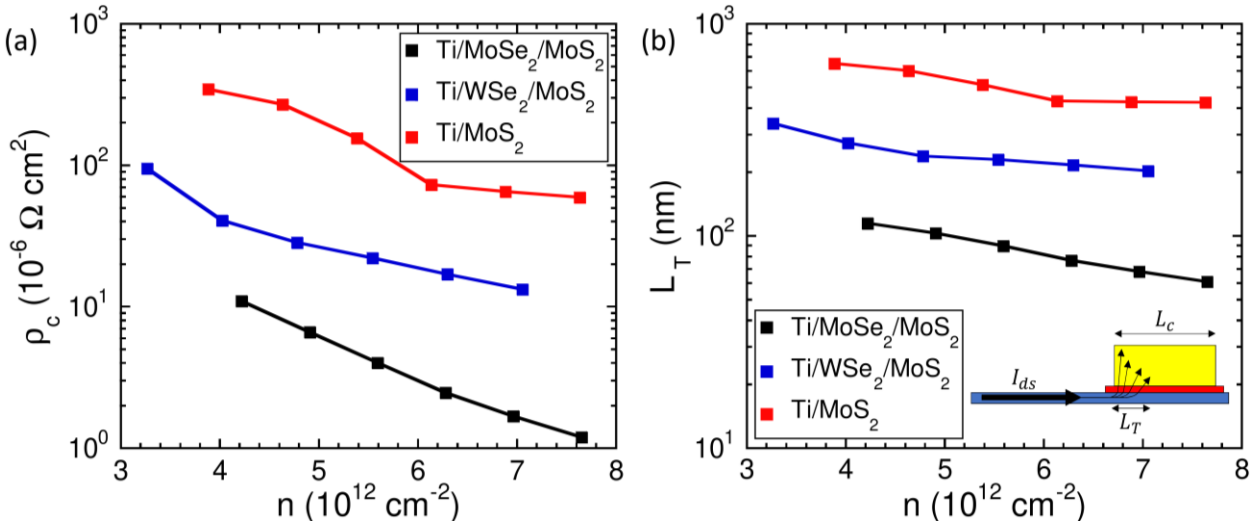

Figure 3.11 Calculated specific contact resistivity and transfer length of MoS_2 FETs. **(a)** Specific contact resistivity and **(b)** transfer length as a function of carrier density calculated from $R_C = (\rho_C/L_T)\,coth(L_C/L_T)$ and $L_T = (\rho_C/R_{sh})^{1/2}$, where R_C and R_{sh} are extracted from the TLM measurements. The **inset** of **(b)** shows an illustration of the decaying current injected over the transfer length. In each contact type, the average contact length (L_C) was 1 μm which is at least several times large the largest transfer length, ensuring that current crowding is not a significant factor in our measurements.

Aside from the method of extracting the current transfer length L_T as shown above by solving the coupled ***equations (3.6)*** and ***(3.7)***, L_T can also be found from the curve of total device resistance as a function of channel length (such as **Figure *3.10 d***). In this method, the current transfer length can be found from the *x*-intercept of the curve fit.[20] In theory, this fitting method should yield a similar value to that found using ***equations (3.6)*** and ***(3.7)*** and reported in ***Figure 3.11(b)***. For a relative agreement between these two calculations, the contact length L_C should be several times larger than the current transfer length L_T. If this relation is not satisfied, then the device will suffer from current crowding at the injection point and an increase in the contact resistivity. The current crowding effect decays exponentially moving away from the contact edge. If there is negligible current crowding in the contacts, then the current transfer lengths found using both calculation methods should agree. However, if current crowding is a significant factor then the two calculation methods should reveal a disparity in current transfer lengths.

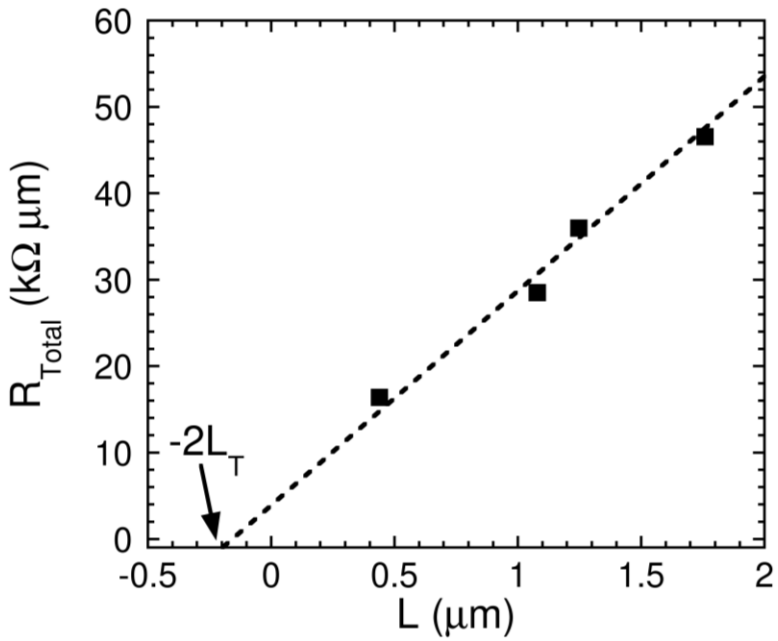

Figure 3.12 Extraction of current transfer length L_T from the total resistance R_{Total} as a function channel length L curve.

To investigate the relative effect of current crowding in these devices with contact lengths of $L_C \approx 1$ μm, ***Table 3.1*** summarizes the current transfer lengths found by each calculation for the three contact types. The table shows two columns for each contact type, one for the current transfer length calculated using ***equations (3.6)*** and ***(3.7)*** and the second for the current transfer length found from the method shown in ***Figure 3.12***. The current transfer lengths found in Ti/$MoSe_2$ and Ti/WSe_2 contacts show near ideal agreement for all gate voltages (carrier densities). This indicates that, while the current transfer length increases as function of decreasing gate voltage, the crowding effect is a negligible factor both contact methods. On the other hand, direct Ti contacts do not exhibit similar behavior. At relatively high gate voltages (V_{gs} = 80 to 60 V) the current transfer length agrees well using both methods. However, as the gate voltage decreases the disparity between each calculated transfer length becomes larger indicating an increasingly pronounced effect of current crowding.

V_{gs} (V)	L_T $MoSe_2$ fit (nm)	L_T $MoSe_2$ calc (nm)	L_T WSe_2 fit (nm)	L_T WSe_2 calc (nm)	L_T Ti fit (nm)	L_T Ti calc (nm)
80	81	79	205	203	445	427
70	93	92	217	216	447	428
60	112	109	233	229	452	433
50	139	138	239	239	561	517
40	176	175	275	274	684	601

Table 3.1 Comparing extracted transfer length from equation solver and the transfer length from fitting. The fitting columns refer to the transfer length extracted from the best fit line when plotting total resistance as a function of channel length. In this method, the *x*-intercept value corresponds to $2L_T$. The calculated columns refer to using a numerical method to solve for both the specific contact resistivity and contact transfer length simultaneously from the equations: $R_C = (\rho_C/L_T)\,coth(L_C/L_T)$ and $L_T = (\rho_C/R_{sh})^{1/2}$. The transfer length found using both the fitting and numerical methods are in agreement for devices using Ti/$MoSe_2$ and Ti/WSe_2 contacts at all gate voltage (carrier density) values. This relative agreement indicates that the chosen contact length ($L_C \approx 1$ μm) is sufficiently large enough to have a negligible effect on the current injection. The transfer lengths found from each method for the direct Ti contacts are consistent at large gate voltage (carrier density) values, but as the gate voltage is decreased the disparity between the parameter extracted from the fit and numerical approach begins to deviate substantially compared to the $MoSe_2$ and WSe_2 interlayer indicating that current crowding may not be negligible for smaller gate voltages in direct Ti contacts.

3.5.3 Temperature Dependent Contact Properties

Figure *3.13(a)* shows the specific contact resistivity in Ti/$MoSe_2$ contacts to MoS_2 as a function of carrier density for several temperatures. As expected, the contact resistivity increases with decreasing temperature due to decreased thermionic emission current. However, it is still relatively small with specific contact resistivity increasing from ~ 1.1×10^{-6} Ω cm^2 at room temperature to ~ 4.5×10^{-6} Ω cm^2 at 180K. In addition, **Figure *3.13(b)*** shows the extracted transfer length for several temperatures. The transfer length increases with decreasing temperature, which is consistent with a decreasing R_{sh} at lower temperatures. As the temperature decreases phonon scattering in the MoS_2 channel becomes less pronounced, which decreases the R_{sh}. While at room temperature the minimum transfer length is ~ 60 nm consistent with a large R_{sh} as the current would

prefers to be injected near the contact edge in a channel with large sheet resistance. Yet, as the temperature decreases, so too, does the sheet resistance, leading to a less resistive layer at the contact interface yielding a larger transfer length.

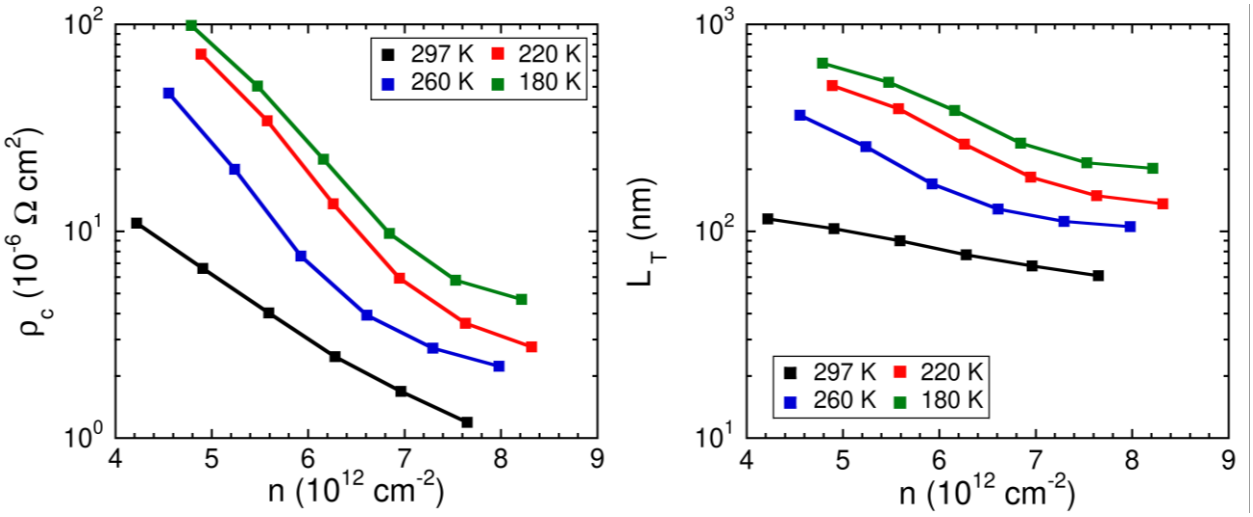

Figure 3.13 Extracted **(a)** Specific contact resistivity and **(b)** transfer length as a function of carrier density at several different temperatures for Ti/$MoSe_2$ contacts to MoS_2.

3.6 Effects of Tunneling Barrier Height and Width

While the addition of an interlayer at the contacts lowers the effective SBH, it also introduces a series tunneling barrier. Here, we examine the influence of tunneling barrier height and thickness on the output characteristics at low temperatures, where thermionic emission is a non-dominant factor. The current through the interlayer exponentially decreases with the tunneling barrier thickness and also the square root of the barrier according to:

$$I_{DS} \propto V_{DS}\ exp\left(-2\Delta s\sqrt{2m^*\bar{\Phi}}/\hbar\right), \qquad (\mathbf{3.8})$$

where Δs is the interlayer thickness, $\bar{\Phi}$ is the tunneling barrier height, and m^* is the carrier effective mass.[72] Therefore, devices with a relatively large interlayer tunneling barrier height (e.g. hBN) should exhibit much lower current; and thick interlayers should also

exhibit this behavior. To minimize the tunneling resistance and thus to maxmize output currents, both the tunneling barrier height and thickness should be minimized. ***Figure 3.14*** compares the output current of different interlayer materials with similar tunneling barrier thickness (~ 2.4 nm) in the low-bias region at low temperature, where the tunneling effect is more pronounced than at room temperature. Because the tunneling barrier height increases in of order Ti/$MoSe_2$/MoS_2 (***Figure 3.14 a***), Ti/WSe_2/MoS_2 (***Figure 3.14 b***), Ti/hBN/MoS_2 (***Figure 3.14 c***; note the different units of current) junctions, the output currents decrease monotonically and also become increasingly nonlinear. Impressively, the device with Ti/$MoSe_2$/MoS_2 exhibits over two orders of magnitidue higher output current than that with Ti/hBN/MoS_2 contacts, inspite of the similar channel and interlayer thicknesses. While the MoS_2 device with Ti/$MoSe_2$ contacts have the lowest tunneling barreir height and lowest SBH, the device with Ti/WSe_2 and Ti/hBN contacts have similar SBHs. This result strongly indicates that lowering the tunneling barreir height is critical to reducing the overall contact resistance.

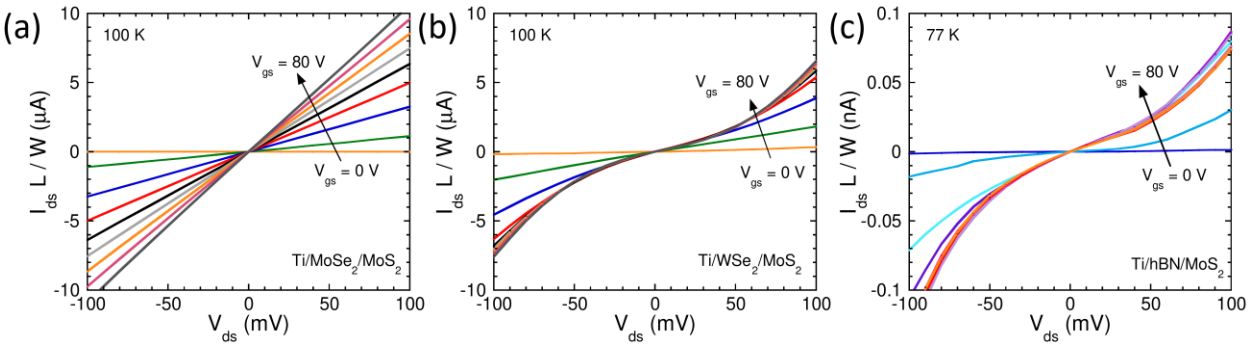

Figure 3.14 Low temperature normalized output current for **(a)** Ti/$MoSe_2$, **(b)** Ti/WSe_2, and **(c)** Ti/hBN (note the different unit of current) contacts to MoS_2 FETs.

Figure *3.15* compares two Ti/WSe_2 contacted MoS_2 devices with different WSe_2 interalyer thickness. As the interlayer thickness increases from ~ 2.4 nm to 5.5 nm, the

output currents decrease by nearly three orders of magnitude (note the different units of current used in **Figure *3.15 a*** and **Figure *3.15 b***).

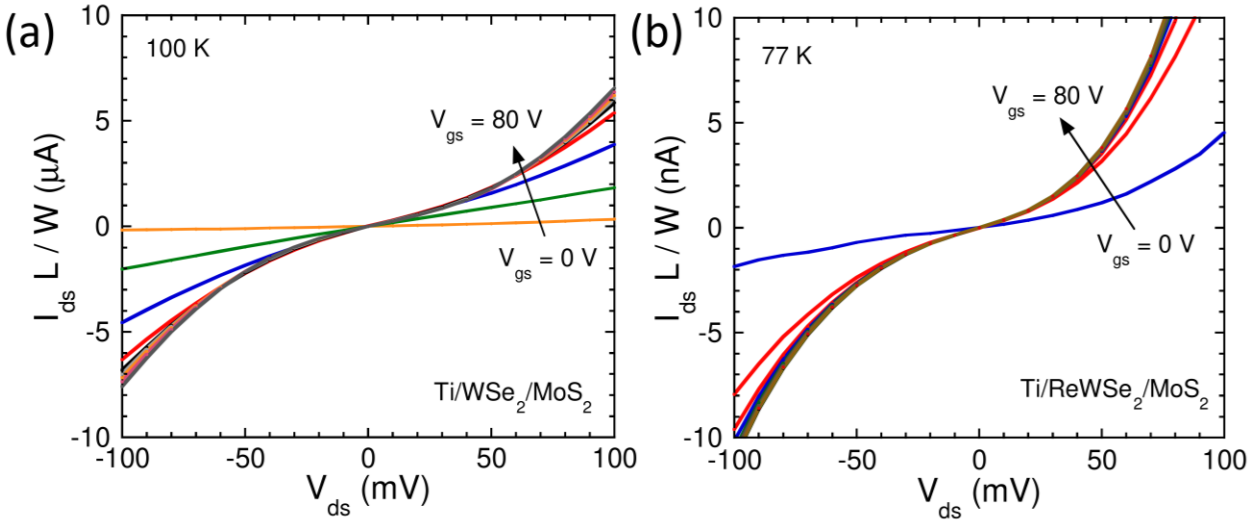

Figure 3.15 Low temperature normalized output current for **(a)** Ti/WSe_2 and **(b)** $Ti/ReWSe_2$ (note the different unit of current) contacts to MoS_2 FETs.

3.7 Contributions of Interlayer Conduction to Device Conduction

Previously shown results in the literature make use of metal-insulator-semiconductor (MIS) structures to reduce the Schottky barrier height (SBH). However, since our metal-semiconductor-semiconductor (MSS) structures use 2D semiconductors inserted between the semiconducting channel and the metal contact, it is non-trivial that the 2D interlayer material does not contribute significantly to the device's drain/source current. Particularly, in our MoS_2 devices used to determine the contact resistance of $Ti/MoSe_2/MoS_2$ ($Ti/WSe_2/MoS_2$) contacts by the transfer length method (TLM), the channel regions are also covered by an ultrathin $MoSe_2$ (WSe_2) layer. ***Figure 3.16*** compares the transfer characteristics of direct Ti contacts to the ultrathin (2~3 nm) interlayer materials used in the main text (WSe_2 and $MoSe_2$) with direct Ti contacts to a MoS_2 channel. The overall contribution of current from the ultrathin interlayer materials in

MoS_2 devices with MSS contacts is nearly 3 orders of magnitude smaller than the current produced in MoS_2 FETs with direct Ti contacts. Therefore, we can conclude that the interlayer materials do not significantly contribute to the overall drain/source current as a parallel channel in MoS_2 FETs with MSS contacts.

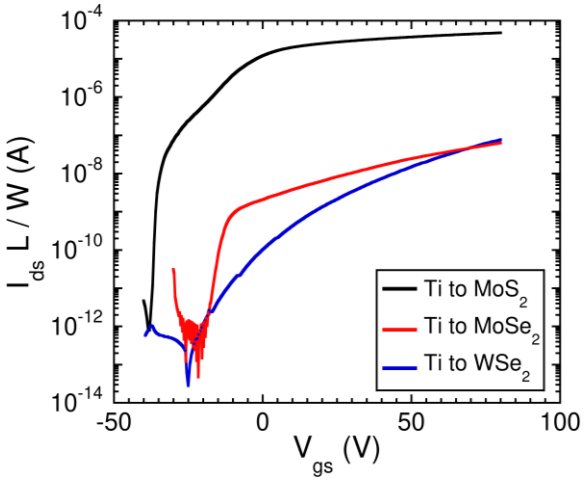

Figure 3.16 Comparison normalized transfer current for direct Ti contacts to MoS_2 (black), $MoSe_2$ (red), and WSe_2 (blue)

3.8 Summary

In this chapter we have introduced a new contact engineering method to minimize the SBH and contact resistivity of MoS_2 FETs by using ultrathin 2D semiconductors as contact interlayers. We demonstrate that the addition of a few-layer $MoSe_2$ between the MoS_2 channel and Ti electrodes reduces the SBH at the contacts by a factor of 4 from ~ 100 meV to ~ 25 meV, contact resistivity by about 60 times from $\sim 6 \times 10^{-5} \Omega\, cm^2$ to $\sim 1 \times 10^{-6} \Omega\, cm^2$, and current transfer length by a factor of 6 from ~ 425 nm to ~ 70 nm. The drastic reduction of SBH can be attributed to the synergy of Fermi-level pinning close to the conduction band edge of the $MoSe_2$ interlayer and the smaller electron affinity of $MoSe_2$ interlayer than MoS_2 channel.

Chapter 4 PERFORMANCE OF 2D INTERLAYER FETs

4.1 Introduction

FETs fabricated with 2D materials such as TMDs have attracted much attention due to their unique material properties that make it possible to scale their channel thickness down to the single atomic layer. This makes them promising candidates for use in next-generation electronics. One of the limiting factors in the exploration of this is their propensity for form a significant contact barrier. In the previous chapter we discussed how inserting a 2D semiconductor interlayer can significantly reduce this barrier and improve the contact resistivity and current transfer length, whose reduction are essential to continued growth and miniaturization of 2D FETs. In this chapter we discuss how the lowered SBH and contact resistivity by using a 2D semiconductor interlayer affects the performance of MoS_2 FETs.

In the development 2D FETs, the performance has been studied extensively. One of the major parameters used to assess device's performance is the carrier mobility, which can be defined as the efficiency with which carriers are transported in a semiconducting material.[95] The mobility is affected by a number of factors, such as interface surface roughness, electron trapping, other structural defects, and non-ideal electrical contacts.[96, 97] Many of the extrinsic factors affecting the device performance have been improved upon since the early days of 2D materials. For example, the use of atomically smooth hBN as a dielectric material greatly reduces interface scattering.[77] To realistically assess MoS_2 FETs the performance must be reliably and consistent and minimizing the contact effects and extrinsic factors are important in this.[98]

4.2 Field-Effect and Effect Mobilities

4.2.1 Field-Effect Mobility

First, the two-dimensional (2D) conductivity is defined as

$$\sigma_{2D} = \frac{L}{W}\frac{I_{DS}}{V_{DS}}, \tag{4.1}$$

where L and W are the channel length and width, respectively, I_{DS} is the drain/source current, and V_{DS} is the drain/source voltage. Then, the field-effect mobility is defined as

$$\mu_{FE} = \frac{1}{C_G}\frac{d\sigma_{2D}}{dV_{GS}}, \tag{4.2}$$

where C_G is the gate capacitance (equivalent capacitance of SiO_2 and hBN substrate).

4.2.2 Effective Mobility

The carrier density is defined as

$$n = C_G(V_G - V_{TH}), \tag{4.3}$$

where V_{TH} is the threshold voltage. In accordance with the Drude model, the effective mobility be found by the 2D conductivity over the carrier density

$$\mu_{eff} = \frac{\sigma_{2D}}{C_G(V_G - V_{TH})}. \tag{4.4}$$

4.2.3 Comparison of Mobilities

In ideal FETs with low-resistance ohmic contacts, the field effect mobility is expected to be consistent with the actual mobility (Drude mobility) of the channel is the mobility is independent of the carrier density. In this case, the slope of 2D conductivity *vs.* gate voltage should also be linear. However, in realistic devices which have a substantial SB present at the metal/semiconductor interface, the field-effect mobility derived from ***equation (4.2)*** is likely to deviate from the actual channel mobility. In some cases, it could even overestimate the mobility as shown in ***Figure 4.1***. This is because in the low carrier

density region the drain/source current is suppressed by the SB. As the carrier density (gate voltage) increases, the SB thickness is quickly reduced, leading to a rapid increase of tunneling and thermally assisted tunneling currents through the barrier. As a result, the transconductance (slope of 2D conductivity *vs.* gate voltage; $(d\sigma_{2D}/dV_{GS})$ can be artificially enhanced, which could result in the overestimation of mobility.

On the other hand, the effective mobility is less affected by this artificially enhancement of trans-conductance. However, in order for the effective mobility to represent the actual mobility, it is important to accurately determine the threshold voltage (V_{th}) corresponding to zero carrier density. In ideal transistors with low-resistance ohmic contacts, the effective mobility should also be consistent with the actual mobility. However, the presence of a significant Schottky barrier not only shift the threshold voltage but also reduce the 2D conductivity. As a result, the effective mobility could also deviate significantly from the actual mobility. Therefore, it is important to extract both the field-effect and effect mobilities. They should be consistent with each other in the case of FETs with low-resistance ohmic (or nearly ohmic) contacts. A discrepancy between the field-effect and effective mobility values extracted from the same device indicates the presence of a significant SB.

Figure *4.1* shows an example of room-temperature transfer characteristics of two MoS_2 FETs with and without $MoSe_2$ inserted at the Ti electrodes using the same MoS_2 channel material. There is a significant threshold voltage shift in the direct Ti metal contacted device due to the large SB present. The field-effect mobility in the high voltage linear region in these devices is substantially larger in the direct Ti contacted device (~ 72 $cm^2V^{-1}s^{-1}$) than in the device with $MoSe_2$ interlayer device (~ 59 $cm^2V^{-1}s^{-1}$) in spite of the lower

normalized current in the former. This is an apparent contradiction and suggests that the field-effect mobility is overestimated in the direct Ti contacted device. The origin of the estimation here can be attributed to the threshold voltage shift due to the strong suppression of drain current at low gate voltage by a large SBH which causes a rapid current increase at higher gate voltage as the SB width is reduced. This results in an increased slope of its transfer characteristic and an overestimation in the field-effect mobility, due to a large SBH that can be reduced by inserting a $MoSe_2$ interlayer between the Ti metal and the MoS_2 channel.[99]

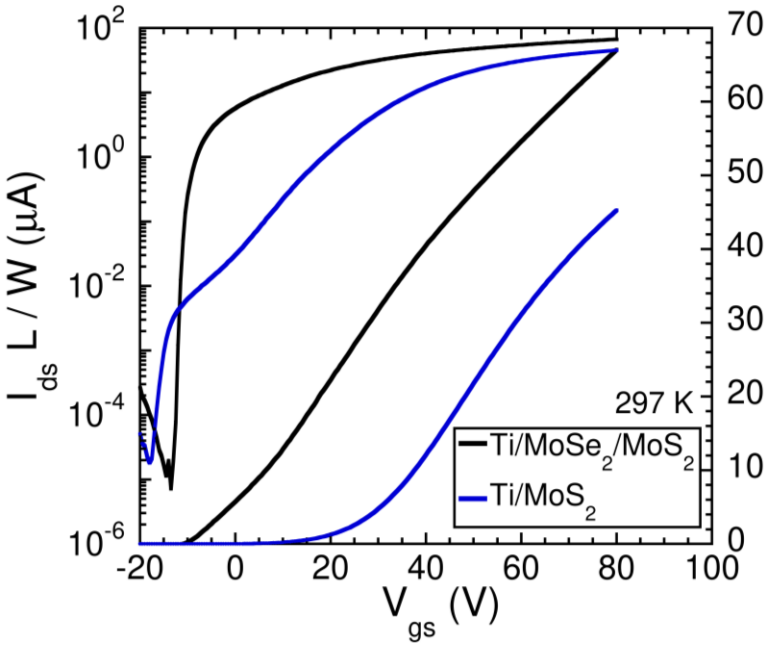

Figure 4.1 Measured room temperature transfer curves comparing FETs with direct Ti and Ti/$MoSe_2$ contacts. The semi-log drain/source current is normalized by device length (L) and width (W) to compare different device geometries. The MoS_2 FET with direct Ti contacts displays a large thermally assisted tunneling region, consistent SB limited contacts resulting in an overestimation of mobility.

Figure *4.2* shows two additional MoS_2 FET devices with Ti/$MoSe_2$ and direct Ti contacts. Similar to the devices shown in **Figure *4.1***, they were also fabricated on the same hBN substrate using the same MoS_2 channel material to rule out any variations in doping concentration or other extrinsic effects. The 2D conductivity is shown as a function

of gate voltage for direct Ti (**Figure *4.2 a***) and Ti/$MoSe_2$ (**Figure *4.2 b***) contacts to MoS_2. Since these devices allow for direct comparison of the transfer characteristics and underlying contact limitation, it is immediately apparent that the direct Ti contacts are limited by a substantial SB due to the large positive shift in its threshold voltage (~ 40 V) as compared to the Ti/$MoSe_2$ contacted device. This large threshold shift in the direct Ti-contacted device is caused by a significant amount of current suppression at low gate voltages ($-20 < V_{gs} < 20$ V) until the thermally assisted tunneling dominates and the current increases rapidly with the gate voltage. The apparent field-effect mobility was calculated in each device to be ~ 71 $cm^2V^{-1}s^{-1}$ in the direct Ti contacted and ~ 50 $cm^2V^{-1}s^{-1}$ in the Ti/$MoSe_2$ contacted MoS_2 devices. This appears to be a contradiction, as the 2D conductivity in the direct Ti-contacted device is nearly a factor of two lower than in the Ti/$MoSe_2$ contacted device. It is expected the overall conductivity should be larger in the device with higher mobility, therefore it can be concluded that the field-effect mobility is overestimated in the direct Ti-contacted device. This mobility overestimation can be explained by the rapid increase of the drain current as the SB thickness is reduced by the gate voltage.

Figure *4.2(c)* compares the effective mobilities of the MoS_2 device with direct Ti and Ti/$MoSe_2$ contacts. When calculating the effective mobility of the device with direct Ti contacts, the threshold voltage of the device with Ti/$MoSe_2$ contacts (~ -20 V) was used as these devices are on the same channel material, we can assume this is close to the true threshold voltage. The effective mobility (~ 30 $cm^2V^{-1}s^{-1}$) of the MoS_2 device with direct Ti contacts is less than half of its field-effect mobility (~ 71 $cm^2V^{-1}s^{-1}$). In contrast, the MoS_2 device Ti/$MoSe_2$ contacts yields field-effect and effective mobilities of nearly

identical values (~ 50 $cm^2V^{-1}s^{-1}$) with a nearly gate-voltage independent effective mobility a high gate voltage. The excellent agreement between μ_{EF} and μ_{eff} in the MoS_2 device with Ti/MoS_2 contacts suggests negligible contact effects. On the other hand, the discrepancy between μ_{FE} and μ_{eff} in the MoS_2 device with direct Ti contacts is a strong indication of a non-negligible SB.

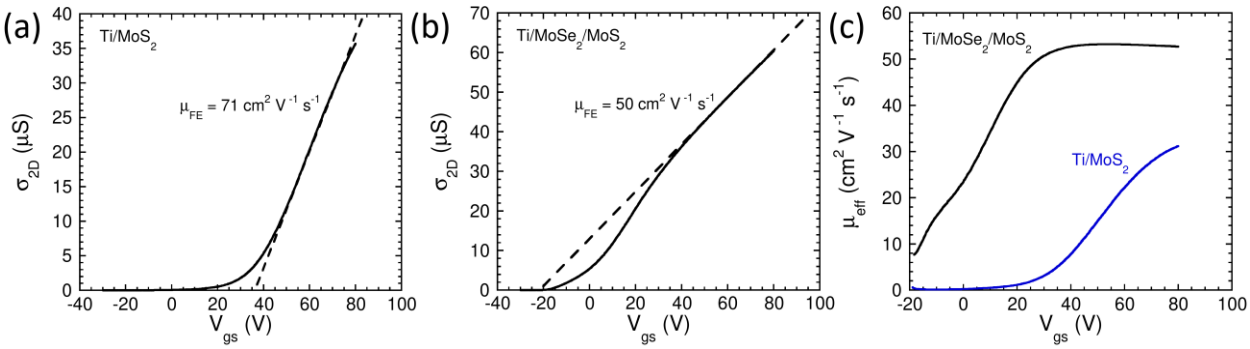

Figure 4.2 Extraction of field-effect mobility from the 2D conductivity curve for **(a)** direct Ti and **(b)** Ti/$MoSe_2$ contacts to MoS_2. **(c)** Comparison of effective mobility for direct Ti (blue curve) and Ti/$MoSe_2$ (black curve) contacts.

The suppression of drain/source current by the SB and the subsequent rapid increase in current results in mobility overestimation. ***Figure 4.3*** shows histograms of extracted field effect **Figure *4.3 panel(i)*** and effective mobilities **Figure *4.3 panel(ii)*** in several direct Ti ***Figure 4.3(a)*** and Ti/$MoSe_2$ ***Figure 4.3(b)*** contacted MoS_2 devices. It is apparent that the mobility overestimation is a consistent issue present in direct Ti contacts due to the large SB present. This results in a wide spread of effective and field-effect mobilities. In each device, the field-effect mobility is significantly larger than the effective mobility, confirming the effect that the SB has in suppressing the drain/source current in the low gate voltage region. Conversely, the effective and field-effect mobilities in Ti/$MoSe_2$ contacted devices are in near agreement. By inserting the interlayer and

thereby reducing the SB and its effect in suppressing drain/source current, the mobilities are no longer overestimated.

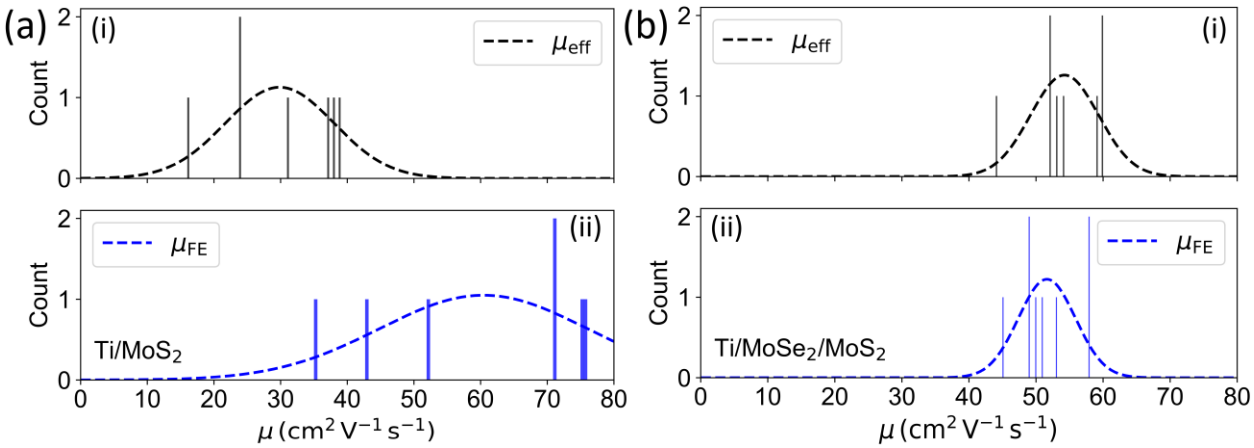

Figure 4.3 Histograms of effective mobility **panel (i)** and field-effect mobility **panel (ii)** in **(a)** direct Ti and **(b)** Ti/$MoSe_2$ contacts to MoS_2 devices.

4.3 Temperature Dependent Transfer Characteristics

To further demonstrate the superiority of 2D interlayer TMD contacts in enhancing the performance of MoS_2 FETs, the electrical transport properties of MoS_2 devices with Ti/$MoSe_2$/MoS_2 and Ti/MoS_2 contacts were studied. **Fig. 6 a, c** presents the temperature-dependent two-terminal conductivity of two MoS_2 devices fabricated on the same uniform MoS_2 flake measured at various temperatures down to 160 K. The two-terminal conductivity is defined by $\sigma = I_{ds}/V_{ds} \times L/W$, where *L* is length W the width of the channel. The main difference between these two devices is that the device in **Fig. 6a** has a 3.8 nm $MoSe_2$ interlayer at the contacts, but the one in **Fig. 6b** is directly contacted by Ti metal. With increasing electron concentration, both devices display a crossover from an insulting regime, where the current increases with increasing temperature, to a metallic regime, where the current decreases with increasing temperature. In addition to a more negative threshold voltage, the insulating regime in the device with Ti/$MoSe_2$/MoS_2

contacts also spans a smaller gate voltage region (- 20 < V_{gs} < 15 V) than that with Ti/MoS_2 contacts (-5 < V_{gs} < 50 V). Because the devices were fabricated from the same uniform MoS_2 flake on the same hBN substrate, the observed differences in the temperature-dependent transfer characteristics can be chiefly attributed to the stronger suppression of drain current by a larger SBH at the Ti/MoS_2 contacts, especially at lower carrier concentrations. As previously demonstrated in **Figure *4.1*,** a strong suppression of the current at low gate voltages and subsequent rapid increase in I_{ds} at higher gate voltages may result in overestimation of field-effect mobility. Therefore, we compare the temperature-dependent effective mobility of the MoS_2 devices with different contacts as a function of gate voltage based on the Drude model: $\mu_{eff} = \sigma_{2D}/C_g(V_g - V_{th})$. In order for the two-terminal effectively mobility to accurately represent the true mobility of the channel, not only the contact resistance needs to be significantly lower than the channel resistance, which is validated in our long channel devices with Ti/$MoSe_2$/MoS_2 contacts by TLM (see ***Figure 3.10***), but also the threshold voltage should occur at zero carrier concentration. The second requirement is fulfilled only when the SBH is negligibly small as in the case of Ti/$MoSe_2$/MoS_2 contacts, where the SBH (~ 25 meV) is comparable to the thermal energy at room temperature. On the other hand, the presence of a substantial SBH of direct Ti/MoS_2 contacts shifts the threshold voltage in the positive gate voltage direction. Therefore, the threshold voltage V_{th} extracted from the device in ***Figure 4.4(a)*** is also used for the device in **Figure *4.4(b)*** to avoid the underestimation of carrier density and thus over estimation of mobility caused by SB induced threshold voltage shift. ***Figure 4.4(c)*** shows that the effective mobility of the device with Ti/$MoSe_2$/MoS_2 contacts is nearly independent of the gate voltage for V_{gs} > 40 V. On the other hand, μ_{eff} in the

device with Ti/MoS_2 contacts keeps increasing with gate voltage until V_{gs} = 80 V as shown in ***Figure 4.4(d)***. This disparity suggests that the true channel mobility is nearly gate independent and that the gate dependence of the effective mobility in **Figure *4.4(d)*** is an artifact caused by a substantial SB at the contacts. Furthermore, the effective mobility of the device with Ti/$MoSe_2$/MoS_2 contacts (160 $cm^2V^{-1}s^{-1}$) is over a factor of 2 larger than that of the device with Ti/MoS_2 contacts at 160 K, which can be attributed to the reduced SBH in the former.

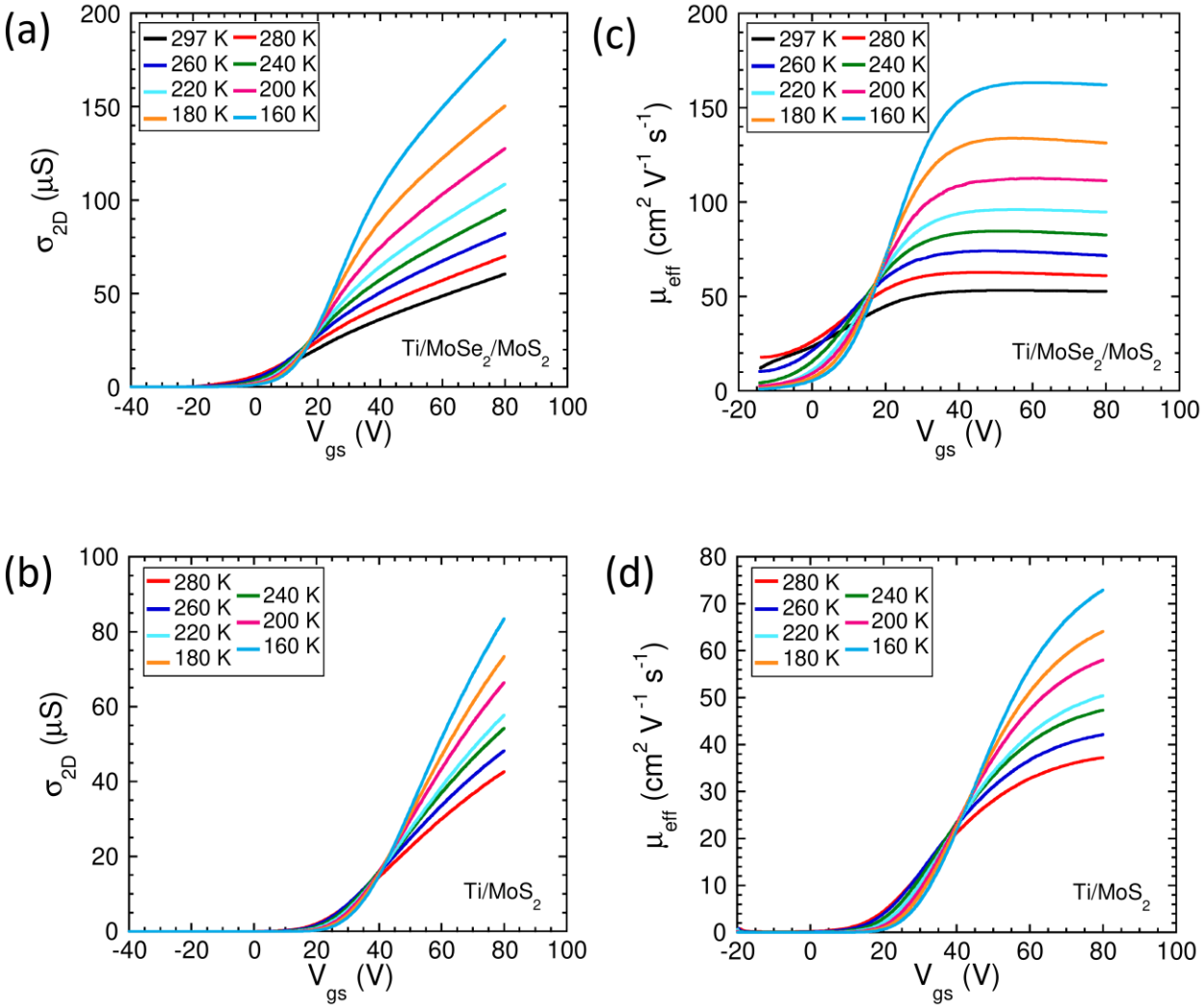

Figure 4.4 Temperature dependent transfer curve measurements and mobility comparison for Ti/$MoSe_2$ interlayer **(a** and **c)** and Ti direct contacts **(b** and **d). (a, b)** 2D-conductivity measured down to 160 K at V_{ds} = 1V. **(c, d)** Effective mobility defined as, $\mu_{eff} = \sigma_{2D}/C_g(V_g - V_{th})$.

Figure *4.5(a, b)* shows the temperature dependence of the mobility at V_{gs} = 80 V. The effective mobility of the MoS_2 device with Ti/$MoSe_2$/MoS_2 contacts follows a $\mu \sim T^{-\gamma}$ dependence with $\gamma \approx 1.8$ in the entire temperature range in good agreement with phonon limited mobility (**see Figure *4.5 a***). On the other hand, the effective mobility of the device with Ti/MoS_2 contacts follows a much weaker temperature dependence of $\mu \sim T^{-1.1}$, indicating that the mobility is increasingly limited by the SB as temperature decreases (see **Figure *4.5 b***). The reason is that the contact resistance in the MoS_2 device with direct Ti contacts constitutes a significant portion of the total resistance of the device, while the contact resistance of the MoS_2 device with Ti/$MoSe_2$ contacts is over an order of magnitude smaller than the total resistance. Moreover, the contact resistance also increases much faster in the former than in the latter due to the larger SBH in the former. For comparison, the temperature-dependent filed-effect mobility in the high gate voltage region is also plotted in **Figure *4.5(a, b)*** to further illustrate the importance of low barrier contacts on the accurate determination of carrier mobility. While the μ_{eff} and μ_{FE} of the device with Ti/$MoSe_2$/MoS_2 contacts are nearly identical, the μ_{FE} of the device with Ti/MoS_2 contacts is larger than its μ_{eff} and follows a stronger temperature dependence of $\mu \sim T^{-1.6}$, indicating that low barrier contacts are essential to accurately extracting the mobilities values and that a non-negligible SBH at the contacts could lead to erroneous mobility values. These SB related artifacts can be eliminated, and the channel limited electrical properties of MoS_2 FETs can be restored by simply inserting a $MoSe_2$ interlayer at the drain and source contacts, which drastically reduces the SBH.

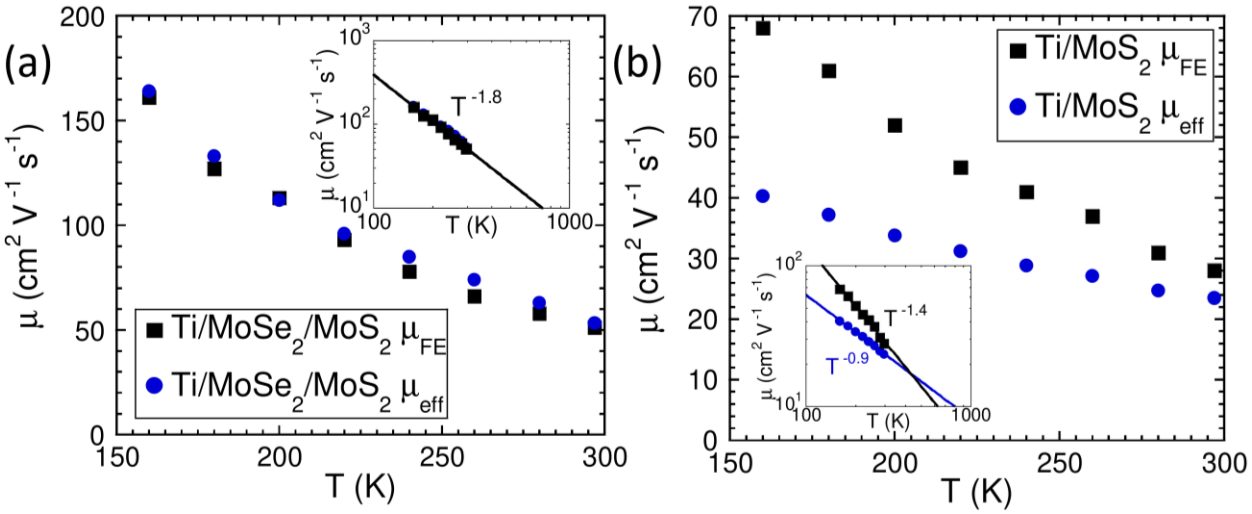

Figure 4.5 Comparison of the field-effect (μ_{FE}) and effective (μ_{eff}) mobilities for decreasing temperatures at $V_{GS} = 80\,V$ for **(a)** Ti/$MoSe_2$ and **(b)** direct Ti contacts to MoS_2.

4.4 Characteristics of WSe_2 Interlayer Contacts to MoS_2 FETs with a Graphite Gate and hBN Dielectric

Add something here about why we use wse2 and not mose2. In order to eliminate the influences of the charge traps in the SiO_2 substrate/dielectric and at the SiO_2/hBN interface, we have fabricated MoS_2 FETs with a graphite gate and hBN dielectric. **Figure *4.6(a)*** and **Figure *4.6(b)*** shows a schematic diagram and optical micrograph of the devices. To account for variations in channel material doping and other extrinsic effects, the device with Ti/WSe_2 contacts was first fabricated (**Figure *4.6 b-i***) then the subsequent direct Ti contacted device was made by extending the metal electrodes into the channel region (**Figure *4.6 b-ii***). Due to the relatively thin hBN dielectric, these devices also exhibit higher gate tunability and improved overall device performance. **Figure *4.6(c)*** and **Figure *4.6(d)*** show transfer characteristics for direct Ti and Ti/WSe_2 contacts to MoS_2 at room temperature. These devices were fabricated using

the same MoS_2 channel to eliminate any variations in doping or gating effects. In **Figure *4.6(c)*** the direct Ti contacts show clear thermally assisted tunneling/tunneling through a SB in the subthreshold region, whereas this behavior is not present in the Ti/WSe_2 contacts. Additionally, the device with Ti/WSe_2 contacts exhibits higher 2D conductivity as well as linear transfer characteristics above the threshold voltage as shown in **Figure *4.6(d)***, suggesting the near absence of a SB and nearly constant mobility. Conversely, the transfer characteristic of the Ti direct contacted device is non-linear with a strongly suppressed current at low carrier densities, which is consistent with the presence of a substantial SB. **Figure *4.6(e)*** and **Figure *4.6(f)*** show the output characteristics normalized by the channel dimensions ($I_{ds} \times L/W$) to account for different device geometries for the Ti/WSe_2 and direct Ti contacted devices, respectively. While both contact methods show linear behavior at high gate voltage, the Ti/WSe_2 contacts show nearly a factor of two larger output current.

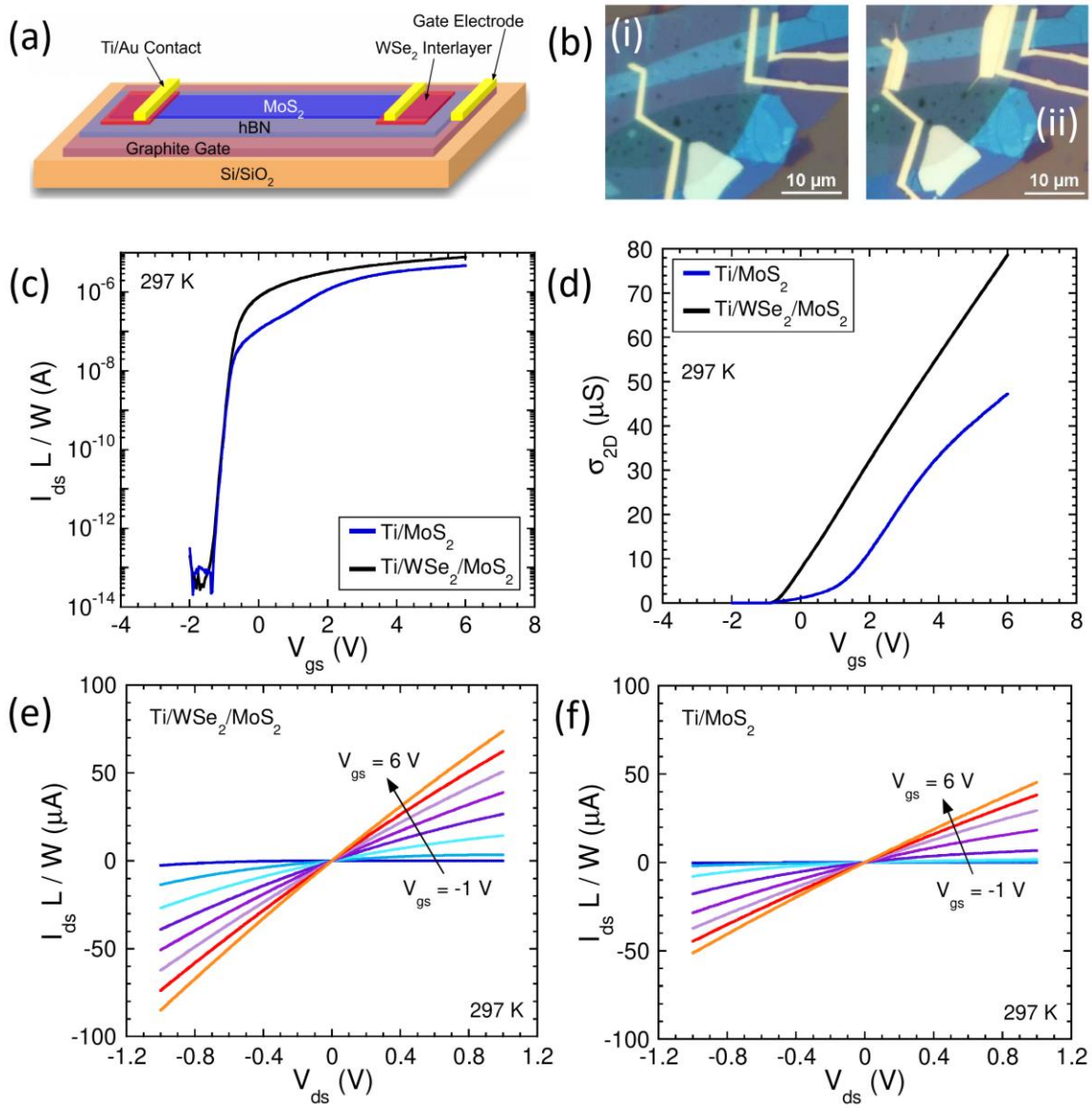

Figure 4.6 (a) Schematic illustration of MoS_2 FET with Ti/WSe_2 contacts fabricated on a hBN dielectric with a graphite gate. **(b)** Optical micrograph of MoS_2 FET on a hBN/graphite stack with **(i)** Ti/WSe_2 and **(ii)** direct Ti contacts. Room temperature **(c)** normalized transfer characteristics and **(d)** 2D conductivity for Ti/WSe_2 (black curves) and direct Ti (blue curves) contacts to MoS_2. Normalized room temperature output curves for **(e)** Ti/WSe_2 and **(f)** direct Ti contacts to MoS_2.

To further elucidate the differences in the contact methods of direct Ti versus Ti/WSe_2 the temperature dependence of each are compared in ***Figure 4.7***. The 2D conductivity of the direct Ti contacts (***Figure 4.7 b***) increases with decreasing temperature, as does the 2D conductivity of the Ti/WSe_2 (***Figure 4.7 a***), as expected.

However, the rate of increase for the Ti/WSe_2 is much larger as compared to the direct Ti contacts (~ 400 μS for Ti/WSe_2 versus ~ 130 μS for direct Ti at 77 K). As the temperature decreases the thermionic emission and thermally assisted tunneling currents also decrease leading to a significant shift in the threshold voltage in direct Ti contacts (~ 2.5 V) while the shift is much less in Ti/WSe_2 contacts (~ 1 V). The normalized output curves of each contact method at 77 K (***inset of Figure 4.7 a*** and ***b***) show that Ti/WSe_2 produces a normalized current of nearly 4 times as large with better overall linearity. Considering the apparent difference in contact quality is also reflected in the effective mobilities of the devices with Ti/WSe_2 (***Figure 4.7 c***) and direct Ti contacts (***Figure 4.7 d***). As temperature decreases the effective mobility increases more rapidly for the Ti/WSe_2 contacts.

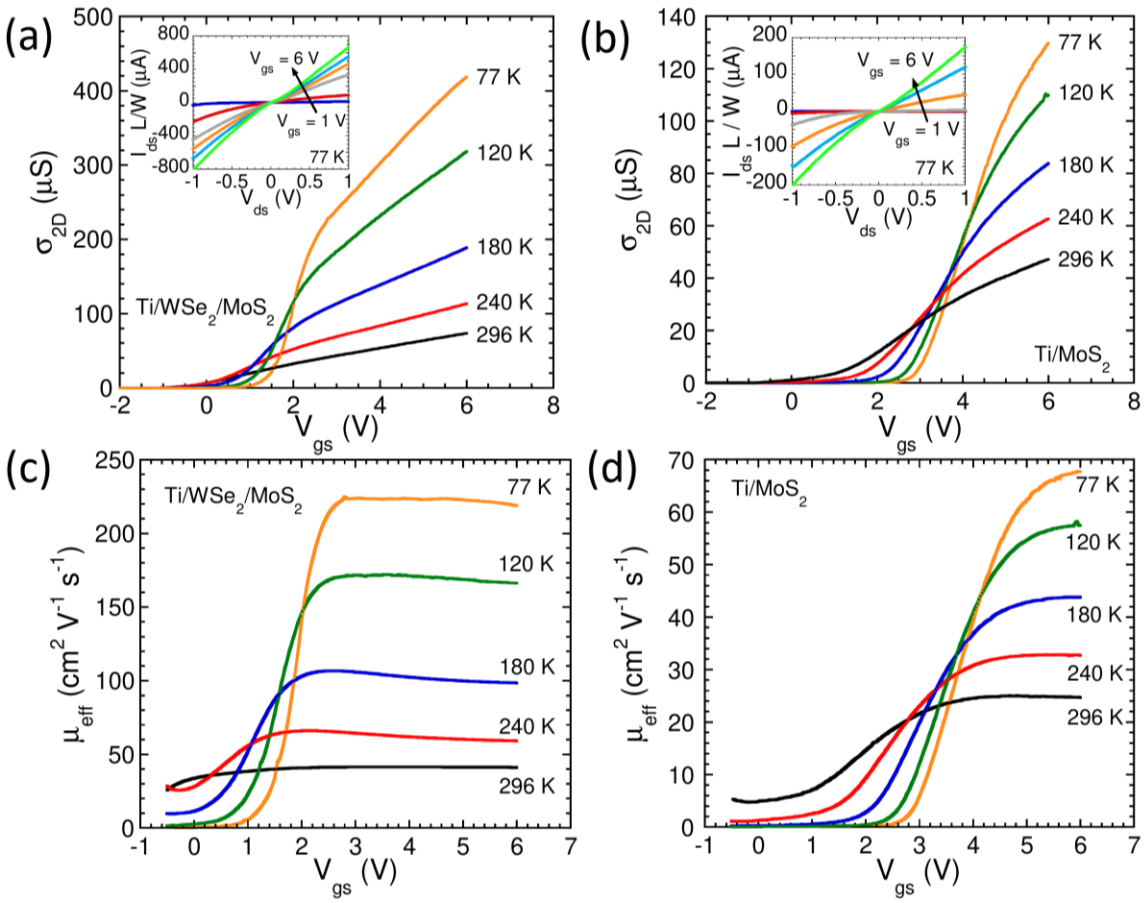

Figure 4.7 Temperature dependent 2D conductivity, low temperature normalized output characteristics (**inset**), and effective mobility for MoS_2 devices with **(a, c)** Ti/WSe_2 and **(b, d)** direct contacts.

Figure 4.8(a, b) shows the temperature dependence of the mobility at V_{gs} = 80 V extracted from the device shown in ***Figure 4.7(a, c)*** with Ti/WSe_2 contacts to MoS_2 using graphite gate with hBN dielectric. The effective and field-effect mobilities both follow a consistent $\mu \sim T^{-\gamma}$ dependence with $\gamma = 1.8$ in the entire temperature range. This number is both, in good agreement with phonon limited mobility and the temperature dependence of the mobilities for MoS_2 devices with Ti/$MoSe_2$ contacts (**see *Figure 4.5 a***).

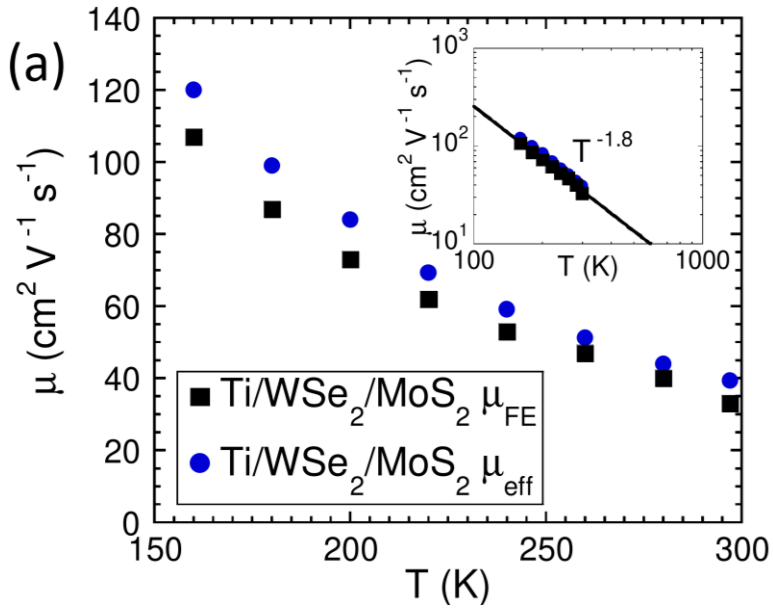

Figure 4.8 Comparison of the field-effect (μ_{FE}) and effective (μ_{eff}) mobilities for decreasing temperatures at $V_{GS} = 80\,V$ for Ti/WSe_2 to MoS_2.

4.5 Improving the Subthreshold Swing

FETs switch from the off-state, where current conduction is minimal, to the on-state, where there is significant current conduction. The region of operation below the threshold voltage is known as the subthreshold region. A FET's ability to efficiently switch from the off-state to the on-state is important for high quality devices. The subthreshold swing (SS) is the amount of gate voltage change needed to change the drain current in the subthreshold by one order of magnitude and is defined as:[3, 100]

$$SS = \frac{\mathrm{d}V_{GS}}{\mathrm{d}(log\, I_{DS})} = ln(10)\frac{\mathrm{d}V_{GS}}{\mathrm{d}(I_{DS})} = ln(10)\frac{k_B T}{q}\left(1 + \frac{C_{\mathrm{it}}}{C_{\mathrm{G}}}\right), \qquad (\mathbf{4.5})$$

where V_{GS} is gate voltage, I_{DS} is the drain current, $k_B T/q$ is the thermal voltage (26 mV at room temperature), and C_{it} and C_{G} are the capacitances of the interface state and gate, respectively. One of the primary factors influencing the *SS* is capacitance of the gate, which is defined as

$$C_{\mathrm{G}} = \frac{\epsilon_{\mathrm{ox}}\epsilon_0}{t_{\mathrm{ox}}}, \qquad (\mathbf{4.6})$$

where t_{ox} is the thickness of the gate dielectric material and ϵ_{ox} and ϵ_0 are the dielectric constants of the oxide material and free-space, respectively. From ***equation (4.5)*** it is evident that a smaller gate capacitance yields a large *SS*. This is illustrated in **Figure *4.9***, where the *SS* at room temperature is shown for two MoS_2 devices fabricated on the same channel material using a 310 nm SiO_2/hBN gate dielectric ($C_{\mathrm{G}} = (1/C_{\mathrm{SiO2}} + 1/C_{\mathrm{hBN}})^{-1} =$ 11.2 nF cm^{-2}). The device shown in **Figure *4.9(a)*** has direct Ti and has a *SS* = 1.34 V dec^{-1}. It is evident by the large thermally assisted tunnel region between the subthreshold region and the on-state that there is a large SB present at the contacts. The device shown in **Figure *4.9(b)*** has Ti/WSe_2 contacts and has a *SS* = 1.29 V dec^{-1}. In this device the thermally assisted tunneling region is absent, suggesting this device is not SB limited. However, the near agreement between the two values of the *SS* in these two devices suggests that the contacts do not limit the *SS*.

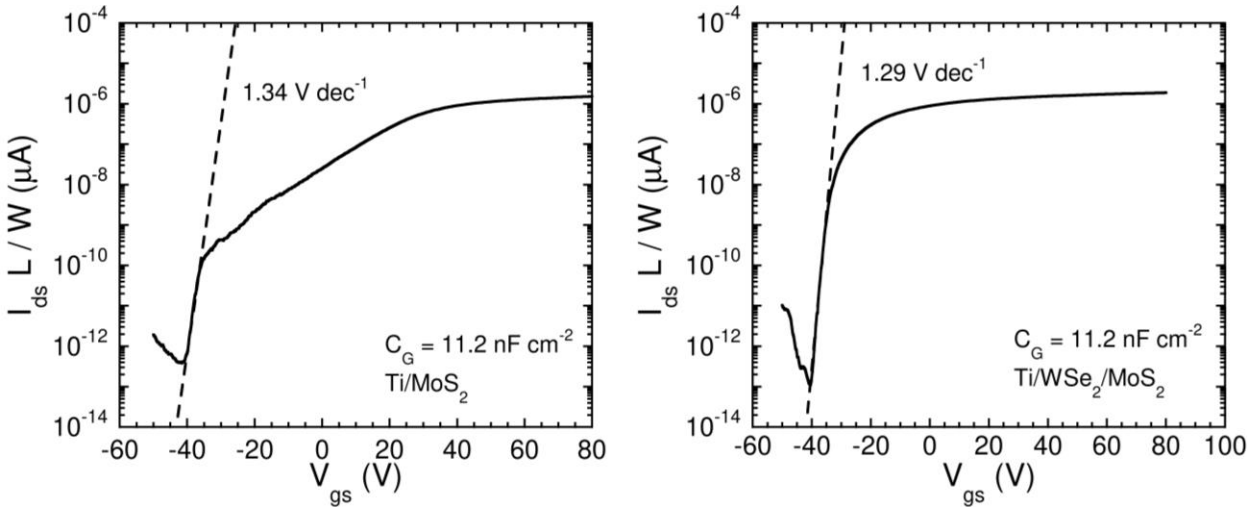

Figure 4.9 Extraction of subthreshold swing (*SS*) at room temperature in MoS_2 FETs fabricated on a SiO_2/hBN dielectric stack with **(a)** direct Ti and **(b)** Ti/WSe_2 contacts.

The current dominant in the subthreshold region is governed by the thermionic injection of electrons over an energy barrier.[6, 51] This injection mechanism implies that

there is a fundamental limit on the steepness with which the FET can switch from the off-state to the on-state. To further decrease the *SS* the interface capacitance must be minimized while the gate capacitance maximized. In this limit where $C_{\mathrm{it}} \to 0$ and $C_{\mathrm{G}} \to \infty$, the room temperature limit of the *SS* is uncovered:

$$\mathrm{SS}_{\mathrm{min}} = ln(10)\frac{k_B T}{q} = ln(10)\frac{k_B \times 300\,\mathrm{K}}{q} = 60\,\mathrm{mV\,dec^{-1}}. \qquad (\mathbf{4.7})$$

Clearly, based on ***equations (4.5)*** and ***(4.6)*** the easiest way to decrease the *SS* is to decrease the dielectric thickness. To achieve this, instead of fabricating devices on a SiO_2/hBN dielectric stack, devices were also fabricated using a graphite gate with a thin hBN dielectric. Using this instead of SiO_2/hBN, the dielectric thickness can be reduced by over an order of magnitude from 310 nm to several nanometers. ***Figure 4.10*** shows the effect reduced dielectric thickness has on the *SS*. By increasing the gate capacitance by about 25 times, the *SS* has decreased from 1.3 V dec $^{-1}$ to 97 mV dec $^{-1}$.

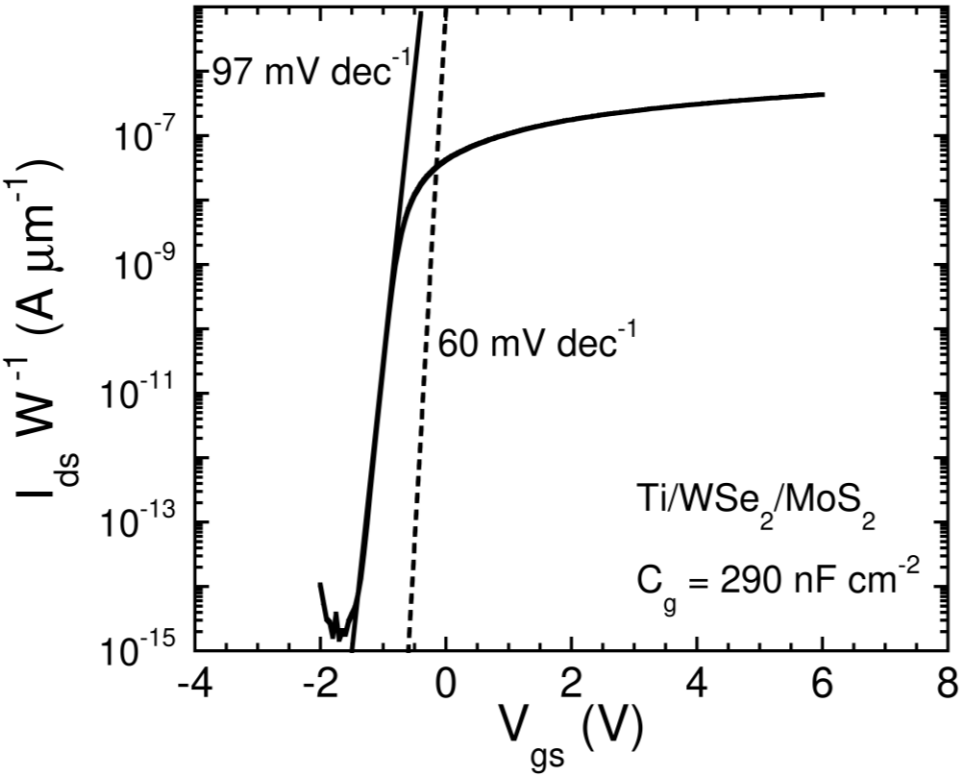

Figure 4.10 Extraction of room temperature *SS* in a Ti/WSe_2 contacted MoS_2 using a hBN dielectric on a graphite gate. The dashed line shows the fundamental limit of *SS* at room temperature for comparison.

According to ***equation (4.5)*** the *SS* should decrease linearly with decreasing temperature. **Figure *4.11*** compares the temperature dependence of the *SS* in a device that uses a graphite gate and hBN dielectric to the fundamental limit. From this it is possible to conclude that further decreasing the dielectric thickness, the limit of *SS* could be approached.

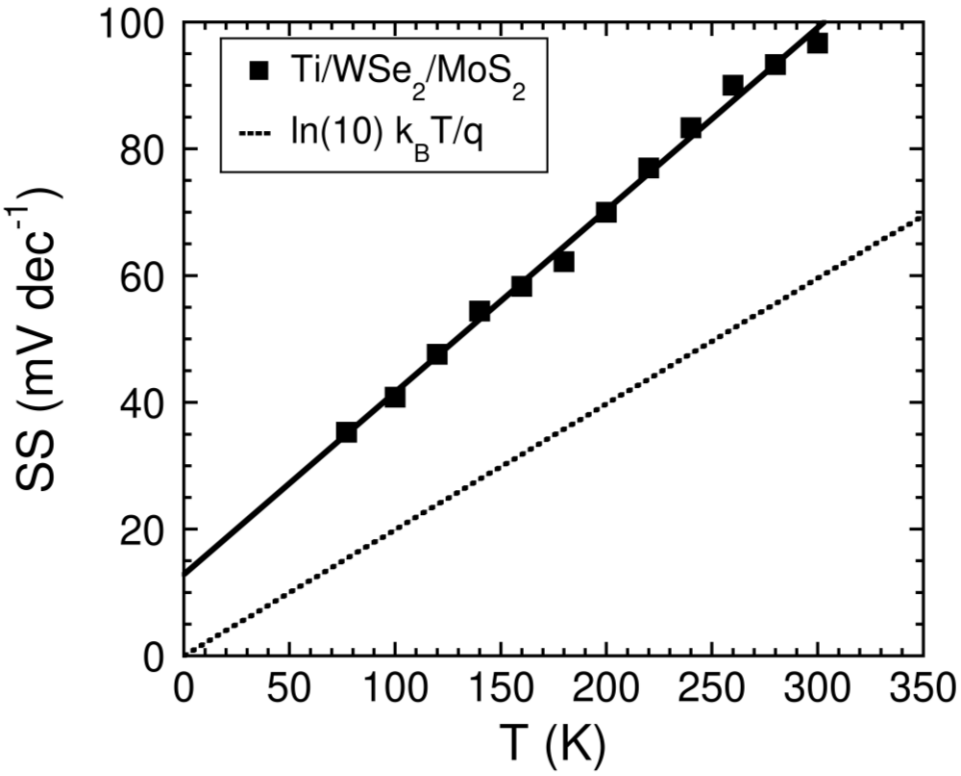

Figure 4.11 *SS* as a function of temperature in a Ti/WSe_2 contacted MoS_2 using a hBN dielectric on a graphite gate. The dashed line shows the fundamental limit of *SS*.

Aside from increasing the gate capacitance, reducing the interface capacitance is also an important factor in reducing the *SS*. From the temperature dependent behavior of the *SS* it is possible to extract the interface capacitance. By plotting the *SS* as a function $ln(10)\, k_B T/q$, the slope is equal to $(1 + C_{\mathrm{it}}/C_{\mathrm{G}})$. Then, from knowing the gate capacitance, the interface capacitance can be found. **Figure *4.12(a)*** shows the *SS* with decreasing temperature for device fabricated on a SiO_2/hBN dielectric stack. Clearly since the gate capacitance in this device is quite small, the *SS* is far from the fundamental limit. **Figure *4.12(b)*** shows the *SS* as a function of decreasing temperature for a device fabricated on a graphite gate with a hBN dielectric. Since the gate capacitance in this case in larger than that on the SiO_2/hBN stack, the *SS* is significantly lower. The interface capacitance in the device on hBN dielectric is 125 nF cm^{-2} while the interface capacitance of the device on the SiO_2/hBN stack is 225 nF cm^{-2}. This suggests that SiO_2 induces a substantial

amount of interface states and charge traps, and using a more atomically smooth surface like hBN as the sole dielectric material will improve the *SS*.

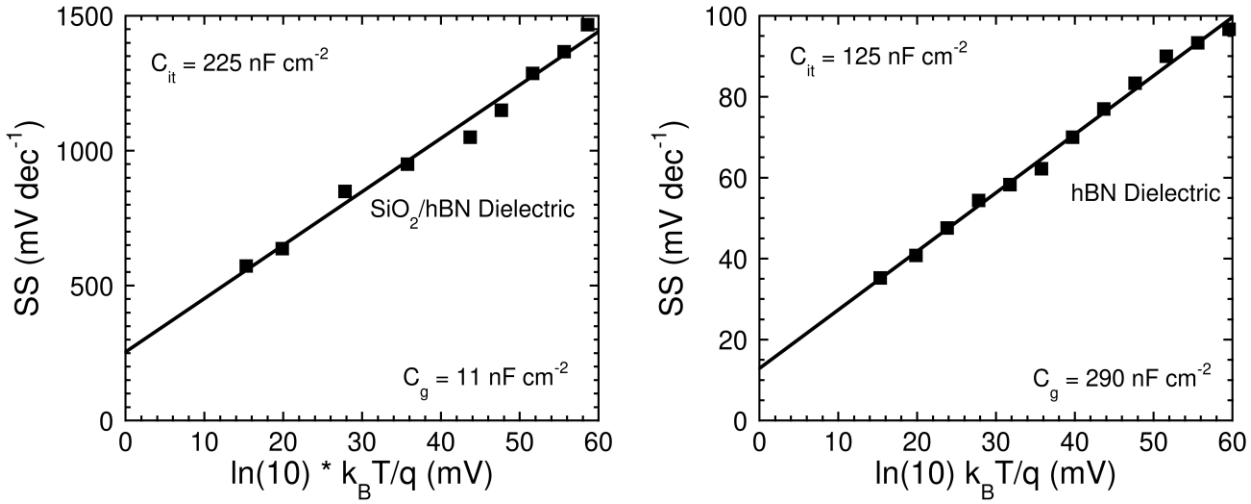

Figure 4.12 Extraction of *SS* as a function as a function of temperature in a Ti/WSe_2 contacted MoS_2 fabricated on a **(a)** SiO_2/hBN stack and **(b)** hBN dielectric on a graphite gate. By extracting the slope of the linear fit, the capacitance of the interface states can be determined.

4.6 Characteristics of Hetero-Layer MoS_2 FETs

To facilitate large scale device fabrication, hetero-layers consisting of different TMDs can be used as the channel material because large scale films of these heterostructures can be grown in large scale (e.g. by chemical vapor deposition). As shown in ***Figure 4.13(a, b)*** the transfer and output characteristic of a FET devices consisting of a $MoSe_2/MoS_2$ hetero-layer channel with Ti as the contact metal closely resembles that of the MoS_2 device with $MoSe_2$ as the contact interlayer at the drain/source regions only (see **Figure *4.1***). ***Figure 4.13(c)*** shows that the effective mobility of the $MoSe_2/MoS_2$ device is nearly gate independent above V_g = 20 V, and comparable to that of MoS_2 devices with Ti/$MoSe_2$ contacts and a bare MoS_2 channel (uncovered by $MoSe_2$). Furthermore, its effective mobility and field-effect mobility also

have nearly identical values (see the inset of ***Figure 4.13 c***). These results suggest that ultrathin $MoSe_2$ in the channel region has little or no effect on the device characteristics.

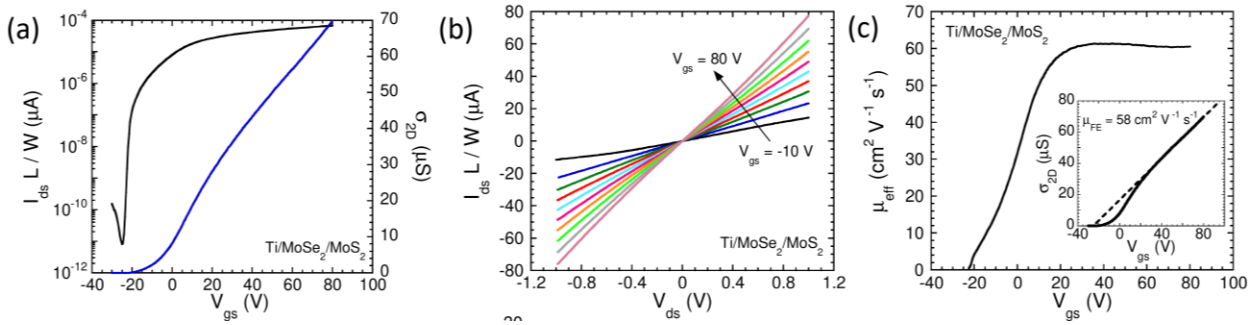

Figure 4.13 Characteristics of a $MoSe_2/MoS_2$ hetero-layer MoS_2 FET with Ti electrodes. **(a)** Normalized linear and semi-log transfer curves of the MoS_2 FET **(b)** Normalized I_{ds}-V_{ds} output curves measured at gate voltages V_{gs} = -10 V to 80V. The output curves are symmetric and linear at all gate voltages. **(c)** Effective mobility and field-effect mobility **(inset)** of the hetero-layer FET. The effective mobility and field-effect mobility extracted from the high gate-voltage linear region are in good agreement.

4.7 Summary

Inserting 2D semiconductor interlayers between the channel materials and the contact electrode greatly reduces the SBH. In this chapter, we have discussed how this reduced SBH leads to enhanced device performance, including high conductivity and mobility. Additionally, by improving the quality of the contacts the problem of mobility overestimation in FETs is addressed. This will allow for a more consistent calculation of the intrinsic transport properties going forward.

Chapter 5 CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

We have developed a new contact method to MoS_2 FETs. Inserting a 2D semiconductor between the channel material and the contact metal greatly reduces the SBH. By strategically choosing the interlayer material, such that the band offset between the channel and the interlayer is minimized, we have minimized the series tunneling resistance that has significantly degraded previous insulating interlayer contact methods. Furthermore, the use of an all 2D material interlayer contact strategy removes the challenges posed from depositing ultrathin oxides on layered TMDs. The resulting SBH by inserting $MoSe_2$ between MoS_2 and Ti contacts is ~ 25 meV, reduced from ~ 100 meV with direct metal contacts. The drastic reduction of the SBH can be attributed to the synergy of FLP close to the conduction band edge of the $MoSe_2$ interlayer and the smaller electron affinity of the $MoSe_2$ interlayer compared to the MoS_2. This SBH reduction works to reduce the contact resistivity 60 times to 1.1 x 10^{-6} Ω cm^2 and the current transfer length down to ~ 60 nm.

The improved contact properties in 2D semiconductor interlayer devices further improves the device performance. Devices with $MoSe_2$ interlayer contacts demonstrate higher and more consistent two-terminal mobility when compared to direct Ti contacts, increasing from ~ 60 $cm^2V^{-1}s^{-1}$ at room temperature to 160 $cm^2V^{-1}s^{-1}$ at 160 K, consistent with phonon limited mobility. We also demonstrate the viability of this method for use in large scale device fabrication through hetero-channel FETs, which can provide potential elegant solutions for scale-up issues in 2D material electronics.

5.2 Future Work

Group VI TMDs have been studied extensively and their properties are well known. Recently, exploration of group X TMDs (noble TMDs) has begun. Palladium diselenide ($PdSe_2$) is one such group X TMD.[101] $PdSe_2$ has a widely tunable, layer-dependent bandgap that ranges from ~ 0 eV in bulk to ~ 1.4 eV in monolayer form coupled with chemical and thermal stability.[102] Initial studies of its electrical properties have shown high room temperature electron mobilities, several times that of group VI TMDs.[102-104] However despite the narrower bandgap, compared to other TMDs, realizing ohmic contacts in $PdSe_2$ has proven quite difficult. Since Pd has more valence electrons (Pd = 10; Mo, W = 6), the extended *d*-orbitals interact strongly with the contact metal resulting in a stronger FLP effect, when compared to group VI TMDs. This manifests in a large SBH, even in relatively thick $PdSe_2$ (i.e. ~ 10 nm) devices as shown in **Figure *5.1***.[105] Furthermore, there is a relative dearth of contact engineering strategies to combat this issue.

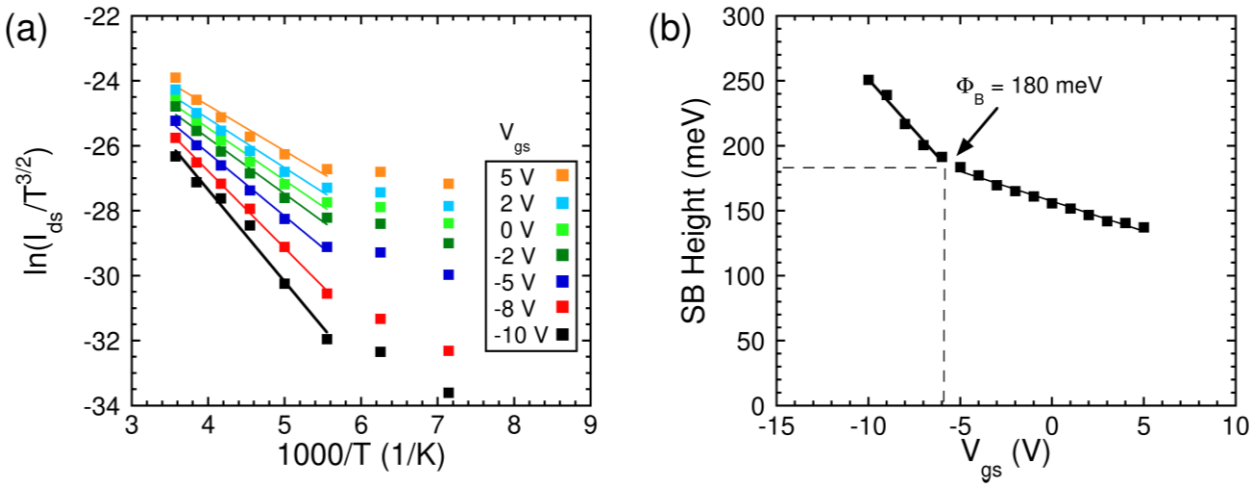

Figure 5.1 Schottky barrier extraction of Ti/Au contacted $PdSe_2$ device. **(a)** The Arrhenius plots for several back-gate bias voltages measured with drain voltage bias at 100 mV. The slope of each curve yields the effective Schottky barrier height at the corresponding gate bias. **(b)** The extracted effective Schottky barrier height at the various back-gate bias voltage, where the flat-band electron Schottky barrier height is measured to be 180 meV.

A potential method for achieving ohmic contact to $PdSe_2$ is the 2D semiconducting interlayer strategy. The narrow bandgap of $PdSe_2$ means there are a number of TMDs that have a favorable band alignment to minimize the series tunneling resistance while simultaneously reducing the interlayer coupling between the channel and the contact metal. By reducing the SBH through this interlayer contact method the intrinsic properties of $PdSe_2$ can be investigated, including improving the carrier mobility and determining the carrier effective mass. In improving the contacts to $PdSe_2$ another goal is to increase the current on-off ratio. Since the bandgap abruptly increases when the material thickness transitions from few-layer to bi-layer and monolayer form, the on-off ratio is expected to increase to > 10^6 in atomically thin $PdSe_2$. To date, on-off ratios of 10^5 have been consistently achieved, but increasing this value has been hampered by the inability to effectively make contacts to ultrathin $PdSe_2$.[102-104] Reducing the contact barrier in $PdSe_2$ FETs will increase the current on-off ratio and carrier mobility, allowing for further assessment of its viability for device applications.

Similar to $PdSe_2$, black phosphorus (BP) is a narrow bandgap 2D material. BP has a bulk bandgap of ~ 0.3 eV which increases to ~ 2 eV in monolayer form.[106] It has a high room temperature hole mobility shown to be > 500 $cm^2V^{-1}s^{-1}$, which has drawn significant attention to its potential device applications.[107, 108] However, BP suffers from oxidation in ambient conditions which degrades the channel material if proper precautions are not taken.[109] Commonly, BP FETs are protected against oxidation by encapsulating or passivating the device using polymers, hBN, or some other similar dielectric material using atomic layer deposition (ALD).[107, 110-115] To further protect against material degradation, FET fabrication in inert environments has been shown to improve quality.[115]

Current contact engineering strategies to reduce the resistance in BP FETs are relatively scarce, primarily consisting of metal work function variation or work function tunable contacts whose effectiveness leaves plenty of room for improvment.[110, 116-118]

Hetero-layer FETs, a FET composed of two layers of 2D materials, where the top layer functions as the 2D interlayer contact and the bottom layer as the channel material. Preliminary results for this structure were shown in ***chapter 4.7***. The ultrathin top layer significantly improves the contact to the channel material through the 2D semiconductor interlayer mechanism while contributing little to overall channel conduction. This device design poses an interesting new direction for making electrical contacts to BP FETs. By fabricating BP hetero-layer FETs with a suitable interlayer contacts in an inert environment, the two major problems in BP FETs can be solved simultaneously. The top layer of the hetero-channel FET will passivate the channel material, preventing oxidation when removed from the inert environment, while also significantly reducing the SBH by through semiconductor interlayer contacts. This new method would offer a reliable, effective, and relatively easy fabrication method to greatly improve the contacts to BP FETs.

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ABSTRACT

IMPROVED CONTACTS AND DEVICE PERFORMANCE IN MoS_2 TRANSISTORS USING 2D SEMICONDUCTOR INTERLAYERS

by

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May 2020

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The rapid growth of modern electronics industry over the past half-century has been sustained by the continued miniaturization of silicon-based electronics. However, as fundamental limits approach, there is a need to search for viable alternative materials for next-generation electronics in the post-silicon era. Two-dimensional (2D) semiconductors such as transition metal dichalcogenides (TMDs) have attracted much attention due to their atomic thickness, absence of dangling bonds and moderately high carrier mobility. However, achieving low-resistance contacts has been a major impediment in developing high-performance field-effect transistors (FETs) based on 2D semiconductors. A substantial Schottky barrier (SB) is often present at the metal/2D-semicondcutor interface, largely due to the Fermi-level pinning effect. To date, various strategies employed to reduce or eliminate the SB and ultimately reduce the contact resistance, such as phase engineering and chemical doping are still deficient. Here, we present a simple, yet effective method to significantly reduce the SB height (SBH) in TMD-based FETs by inserting ultrathin 2D semiconductors as an interlayer at the semiconductor-metal interface. Specifically, we have observed a drastic reduction in the

SBH from ~ 100 meV to ~ 25 meV by inserting an ultrathin $MoSe_2$ between the MoS_2 channel and the contact metal. This improvement can be attributed to the coupling of Fermi-level pinning close to the conduction-band edge of the interlayer and the slightly smaller electron affinity of the $MoSe_2$ interlayer compared to that of the MoS_2 channel. Consequently, this reduction in the SBH results in over an order of magnitude decrease in contact resistivity (from ~ 6×10^{-5} Ω cm^2 to 1×10^{-6} Ω cm^2) and current transfer length (from ~ 425 nm to ~ 60 nm). The improvements in the contact properties yield greater device performance, enhancing the two-terminal mobility from ~30 $cm^2V^{-1}s^{-1}$ to ~ 60 $cm^2V^{-1}s^{-1}$ at room temperature and from ~70 $cm^2V^{-1}s^{-1}$ to ~ 160 $cm^2V^{-1}s^{-1}$ at 160 K. This new contact engineering method presents an important advantage over previous works that utilize insulating interlayers because this method uses advantageous band alignments to reduce the SBH while minimizing the tunneling barrier at the contact interface.

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3. "Reversible Photo-Induced Doping in WSe_2 Field-Effect Transistors." Xuyi Luo, **Kraig Andrews**, Tianjiao Wang, Arthur Bowman, Zhixian Zhou, and Ya-Qiong Xu. *Nanoscale*, *11*(15):7358-7363. 2019.

4. "High Performance WSe_2 Phototransistors with 2D/2D Ohmic Contacts." Tianjiao Wang, **Kraig Andrews**, Arthur Bowman, Tu Hong, Michael Koehler, Jiaqiang Yan, David Mandrus, Zhixian Zhou, and Ya-Qiong Xu. *Nano Letters*, *18*(5):2766-2771. 2018.

Presentations

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